ENHANCEMENT OF TIMING ACCURACY AND WAVEFORM QUALITY IN HIGH PERFORMANCE ASIC TEST AND VERIFICATION SYSTEMS

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ABSTRACT

This thesis reviews design, test, and verification aspects of Application-Specific Integrated Circuits (ASIC). A means of improving edge-placement accuracy and waveform quality in high speed, high performance, ASIC test and verification systems has been developed. Its aim is to minimize timing skew, maintain signal integrity at the Device Under Test (DUT), and actively reduce waveform distortions caused by uncertain DUT loading and transmission path imperfections.

Frequency Domain Reflectometry (FDR) is used to measure voltage reflection coefficients of both the load (DUT) and Pin Electronic Card (PEC) ends of the transmission path. Time domain waveform is obtained using Discrete Fourier Transformation (DFT).

Two prototypes, single and dual directional couplers, have been designed and implemented using Thickfilm-Hybrid Technology (TFH). Both couplers employ strip transmission line structures which support a Transverse Electromagnetic (TEM) propagation mode. FDR experimental results indicate that a matched dual directional coupler can be used in such an application, yielding results comparable to those obtained from an automatic network analyzer.

The path between the PEC and the DUT is modelled using a signal flow graph (SFG) technique. The model contains both lumped, and distributed circuit elements, each of which is represented by scattering parameters. Load models that represent the DUT or PEC receiver are obtained through a direct search optimization algorithm. This thesis implements two such algorithms, the pattern search and simplex algorithms, based on an example load model.

A technique to compute compensation waveforms for linear transmission paths has been developed. Two examples, matched and mismatched channels, are presented. Simulation results show that compensation waveforms computed from the channel characteristic almost completely correct edge-placement timing errors and greatly reduce reflection effects. Implementation of compensation waveforms by simple hardware is possible, leading to edge-placement correction which is almost as good as that obtained from a theoretically computed compensation waveform.

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PREFACE

Since the transistor was invented at Bell Labs in 1947 and the first integrated circuit was made by Texas Instruments in 1959, the first discrete semiconductor tester was not produced until 1960. During the early-seventies attention was paid to testing of semiconductor memory but this was reduced because the emergence of LSI devices in the mid-seventies started to have a significant impact. New topics such as microprocessor testing, design for testability, reliability, and test facilities and techniques started appearing. The test problems became more challenging and rapidly increased in complexity since the introduction of VLSI in 1980s.

However, the microelectronic revolution was not only generating new test problems, it was also creating the means to solve them. The computer-controlled ATEs became practicable with MSI and LSI devices. At the same time, the trend in design of electronic systems was to ever more digital solutions, with the result that the amount of test pattern needed to test them soon required automatic generation. Simulators began to be developed for circuit design, fault simulation, and test pattern generation.

The speed and complexity of the new digital circuits increasingly demanded the efficiency of the simulators and the ATEs' performances. This still continues to the present day. From the hardware view point, IC testers generally lag behind the devices they are required to test by at least one generation. Test technology has been progressing to highly sophisticated levels. Testers with state-of-the-art specifications are being offered by ATE manufacturers. However, the ultimate performance of these testers is not achieved mainly because of the interfacing problems, particularly between the tester and the device being tested.

The author started working on this research under Mr. L. N. M. Edward in 1988. The work continued from the proposal "VLSI Testing Interface" developed by Edward in 1984. The original proposal was aimed at developing a low cost, high performance ASIC prototype verification tester.

In this study, the main emphasis has been paid to developing a means of improving tester-DUT interface. Edge-placement accuracy and signal quality are major targets to be investigated in this thesis.

The title of this thesis indicates the purpose of this study. The word *enhancement* was chosen because the approach developed here is not aimed at replacing conventional

calibration systems. Although the technique described in this thesis can be applied to any high performance IC tester, the acronym ASIC remains in the title to retain the original intention (to develop an ASIC verification system).

Chapter 1 describes the motivation of this research and introduces design, test, and verification aspects of digital Application-Specific Integrated Circuits (ASIC). Classification and comparison of ASIC and standard IC give some indication of testing difficulty for ASIC designers. Advanced Computer-Aided-Design (CAD) tools allow IC design to be highly complex. Today's design complexity requires testing strategy to be considered during the design phase. Computer-Aided-Test (CAT) supports designers with Design for Testability (DFT)[1] tools and some capability to develop test vectors. Test definition and techniques are described to illustrate testing processes during IC manufacture. Finally, the device technologies and their packaging requirements are discussed.

Chapter 2 provides some history and the development of Automatic Test Equipment (ATE) up to the present day. Designing a test head is one of the most critical tasks in tester design. Basic structures and architectures currently employed in most VLSI testers are described. The author then continues to discuss the interface problem between the device and tester which motivated this research. Transmission line analysis is becoming important in high speed digital systems. Major parameters for signal propagation in such systems are presented. Finally, the desirable capability of an IC tester is outlined.

Chapter 3 begins with a discussion on timing accuracy in modern IC testers. Then the proposed approach to improve edge-placement accuracy and waveform quality is presented.

Chapter 4 describes some commonly used transmission line types. Basic concepts in complex impedance measurements are introduced in this chapter. Topics such as signal flow graph (SFG) analysis, network representation, and some useful SFG reduction techniques are outlined.

Chapter 5 presents fundamental theory of electromagnetic directional couplers, and defines their essential parameters. The directional coupler's responses in both steady-state and transient excitation are next presented; then follows the detailed design and implementation of two Thickfilm-Hybrid (TFH) prototypes. The prototypes' characteristics, in the form of scattering parameters, are used to compare performance with a commercial directional coupler.

Chapter 6 concerns the Frequency Domain Reflectometry (FDR) experiment which is aimed at demonstrating the reflectometer technique using the prototype directional couplers. The measurement configuration is first described, then the results are presented for three sets of terminations; capacitor, inductor, and resistor. Finally, a discussion on the experiment results concludes this chapter.

[1]This acronym is used for both "Design for Testability" and "Discrete Fourier Transformation". There should be no ambiguity since these two phrases appear in different contexts.

Chapter 7 describes two optimization techniques, the pattern search of Hooke and Jeeves and the simplex algorithm of Nelder and Mead, implemented to study the feasibility of using direct search optimization methods to determine the load model for the DUT and PEC receiver. The two chosen algorithms are demonstrated based on an example load model. Results and performance comparisons are presented for 20 cases of different initial trial points.

Chapter 8 investigates a technique to compute a compensation waveform for given channel and load characteristics, assuming they can be approximated by a linear time-invariant model. This method models the transmission path between the PEC and DUT using SFG analysis.

The investigation has progressed to the simulation level using SPICE version 2G.6 and simulation results are given for the two example cases of matched and mismatched channels.

Chapter 9 summarises the results obtained from this study and suggests direction for further research.

Two papers have been written as a result of this research:

CHAROEN, B. and EDWARD, L.N.M. (1991), 'Adaptive Enhancement of Timing Accuracy and Waveform Quality in High Performance IC Testers', accepted for publication in *IEEE Transactions on Circuits and Systems*, (scheduled to be published in Vol. 39, No. 2, February 1992).

EDWARD, L.N.M. and CHAROEN, B. (1990), 'On Improving the Edge Placement Accuracy and Signal Quality in USIC Testers', In *The* 9^{th} *Australian Microelectronic Conference Proceedings*, IREE Australia, Adelaide, South Australia, pp. 333–338.

CHAPTER 1

DESIGN AND TEST OF ASIC

This chapter begins with the motivation and main goal of this research, section 1.1. An overview of design, test, and verification of Application-Specific Integrated Circuits (ASIC) is given in sections 1.2 to 1.5 to introduce basic concepts and requirements of digital ASIC testing.

Section 1.2 describes a classification of digital logic integrated circuits (ICs), a comparison between standard and application-specific ICs, and where and why IC testers are needed.

Section 1.3 emphasizes the relation between design and test of an ASIC. The roles of design engineer and test engineer have changed during the last decade in response to testing problems. The relationship between these two disciplines must be improved to reduce time-to-market and therefore increase profit. Test definition and methodologies are presented in section 1.4. Understanding of device process technologies and their package limitations is important for test results to be meaningful. Section 1.5 addresses major IC logic families and briefly reviews available packaging technologies.

1.1 THE PROPOSAL

With ASICs, the *designer* must thoroughly evaluate the foundry prototype before committing to production, which demands a tester offering affordable test verification and test vector development capabilities.

Production testers emphasize go/no-go throughput in volume manufacture, whereas prototype testers provide enhanced diagnostics with no call for volume throughput. Relatively short ASIC design cycles, frequently low production volume, and potentially inexpensive testing if Built-In Self-Test (BIST) is incorporated, suggest that many firms could receive packaged but untested devices from the foundry and never require more than a prototype tester.

Similar needs arise in academic and research organisations. The research reported in this thesis originated from a proposal for an inexpensive "VLSI Testing Interface" [EDWARD, 1984]. This system targets design verification of both full custom and semicustom ASICs. Favourable market prospects predicted by DEWE [1985] failed

to convince potential New Zealand investers and the proposal lapsed. Meanwhile, worldwide research has resulted in similar high performance ASIC testers costing about 20 to 30% of a production tester.

Research directed towards improving tester performance [GARCIA, 1984; COHEN, 1986; JONES, 1987; MUETHING and SAIKLEY, 1987; BRANSON *et al.*, 1988; TSAI and HECHTMAN, 1988; BRANSON, 1989; BRYSON, 1989], has resulted in dramatic improvements. Major tester components, such as the high speed Pin Driver, comparator, programmable time delay and programmable loads, have been developed to an acceptable state and are available as ICs [TUNICK, 1987; WEISS, 1987; GOTSCHEWSKI and SCHWEBER, 1989]. However, there is widespread disagreement about the limits on measurement speed and accuracy. Subnanosecond timing accuracy is today's promise, but can it be achieved? Many tester timing specifications are derived without taking adequate account of test fixtures and the device being tested. In this thesis, these aspects are investigated.

Our main goal is to develop a method of improving timing accuracy and waveform quality which have been corrupted by test fixtures and the device loading effects, and apply this new methodology to the design of the test head of an ASIC test and verification system.

1.2 ASIC: DESIGN AND TEST

Testing is always an integral and vital part of the IC manufacturing processes. Not testing at all would be catastrophic, test cost is proportional to test complexity, and exhaustive testing is usually impossible, especially for a high level of integration (LOI) device. A compromise must be struck between the cost of testing and cost of reworking faulty modules.

An IC involves the fabrication of thousands of components and interconnections at once by a common set of manufacturing steps. Its advantages are reduced system cost, better performance, and greater reliability. These advantages would be lost unless they were tested economically [AGRAWAL and SETH, 1988].

Testing is not used just to exercise the devices and prove their functionality; it is also used to determine their operating limits and performances. One of the major roles of testing is to classify working circuits into several operating ranges. This places a demand for tight specifications and high accuracy testers.

1.2.1 IC Design Methodologies

IC design methodologies may be classified into two alternatives; standard ICs, or application-specific ICs, as shown in Figure 1.1. Although there is no universally accepted method of classifying logic ICs, this classification is intended to clarify the aim of this research.

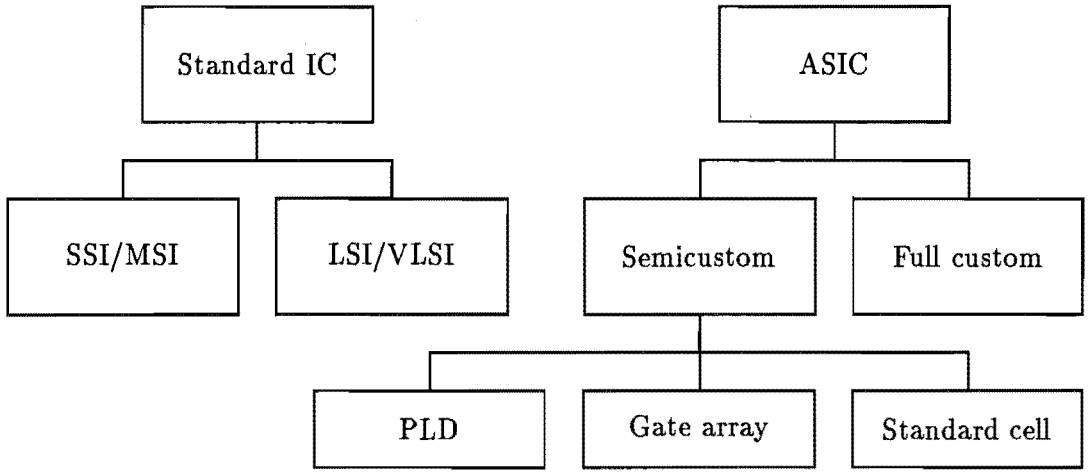


Figure 1.1 Classification of digital logic ICs.

Standard ICs refer to those devices, such as CMOS 4000 or TTL 7400 series, which are commercially available from IC vendors whereas ASICs refer to all the user-designed devices. The acronyms SSI (Small Scale Integration) or VLSI (Very Large Scale Integration) indicate the device complexity rather than transistor-count. However, the transistor-count is often used as a means of classification.

The design of a microelectronic circuit to a particular customer's requirement can be divided into the two broad categories: full custom and semicustom [HURST, 1985]. The terms *full custom* and *semicustom* take various meanings in the literature on microelectronic design. In the full custom approach the objective is to produce the most efficient final design-on-silicon possible within given time and cost constraints. Semicustom uses more expeditious means of design than full custom, namely standard cell, gate array or programmable logic devices (PLD). A comparison of these techniques is described elsewhere [HURST, 1985; MURRAY and REEKIE, 1987].

The acronyms ASIC and VLSI will be used interchangeably throughout this thesis. When the term VLSI is used, the author refers to an ASIC with level of integration equivalent to a VLSI chip. Although this research is aimed at ASIC testing aspects, most techniques described in this thesis can be equally applied to commodity IC testing problems.

1.2.2 ASIC v/s Standard Devices

The introduction of hierarchically-structured design methodologies and the emergence of Computer-Aided-Engineering (CAE) workstations have greatly reduced design time and allowed vast expansion of IC complexity. Numerous Computer-Aided-Design (CAD) tools have been developed to assist designers with simulation and verification of the various design functions. There are many exellent text books on digital IC design particularly for LSI/VLSI devices, for instance [MEAD and CONWAY, 1980; MAVOR

et al., 1983; BENNETS, 1985; PUCKNELL and ESHRAGHIAN, 1988].

1.2.2.1 ASIC features

ASICs are being used more and more by designers who previously designed systems using standard ICs. It has been shown that products using ASIC devices cost less than those containing combinations of standard SSI, MSI, LSI, or VLSI devices [FEY and PARASKEVOPOULOS, 1987]. In addition to the financial advantage, ASICs posses the following desirable features:

- Design security
- Better performance, such as higher speed and lower power dissipation
- Reduction in the number of interconnections in the system, therefore improved reliability
- Small and light weight

ASICs differ from standard devices in many respects:

- Rapid design cycle
- Short product lifetimes
- Small production-lot sizes
- Design diversity
- Rapid design changes
- Uncertainty of achieving production status
- Variety of package types
- High complexity
- High pin-count

Each of these factors has an impact on test methodologies and test equipment. The solution to this problem must come from better integration of CAE and Automatic Test Equipment (ATE).

1.2.2.2 Tools for a testable design

Tools have been developed to help a designer design a testable circuit. They are Computer-Aided-Test (CAT) tools, and can be divided into two groups: Design For Testability (DFT) and Automatic Test Pattern Generation (ATPG). DFT tools help in the design of more testable circuits while test pattern generation involves a search for

a sequence of input vectors that cause relevant faults to be detected on the primary IC outputs. A full-coverage vector set results in long test times and for most complex ICs is impossible to generate. ATPG incorporating fault simulation and testability analysis helps the test engineer generate sufficient fault-coverage vectors to evaluate his designs. Figure 1.2 shows a flow chart of an ASIC design cycle using CAT tools.

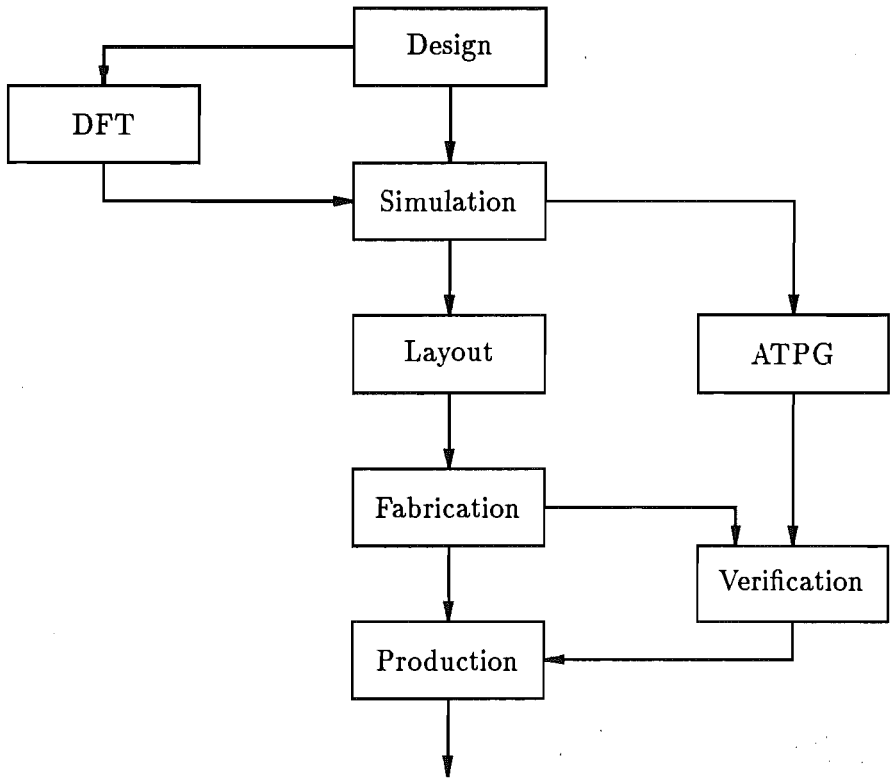


Figure 1.2 Flow chart of ASIC design cycle using CAT tools.

1.2.3 Where Testing is Performed

Figure 1.3 shows the various places in the IC manufacturing process where testing is performed [McMINN, 1985]. Although some testing (mainly on the process itself) is done during device fabrication, most device testing is performed after the semiconductor wafers have been fabricated.

ICs are tested at least twice during manufacture: before wafer-scribing and die-separation, and after packaging. The first is used to distinguish between potentially good and clearly defective semiconductor circuits. Defective circuits are usually inked at this point. The wafer is scribed and cut, and the potentially good devices are collected and packaged.

For new designs the next step is a characterization test, where the devices are tested under specified stresses for their operating and electrical limits. This results in

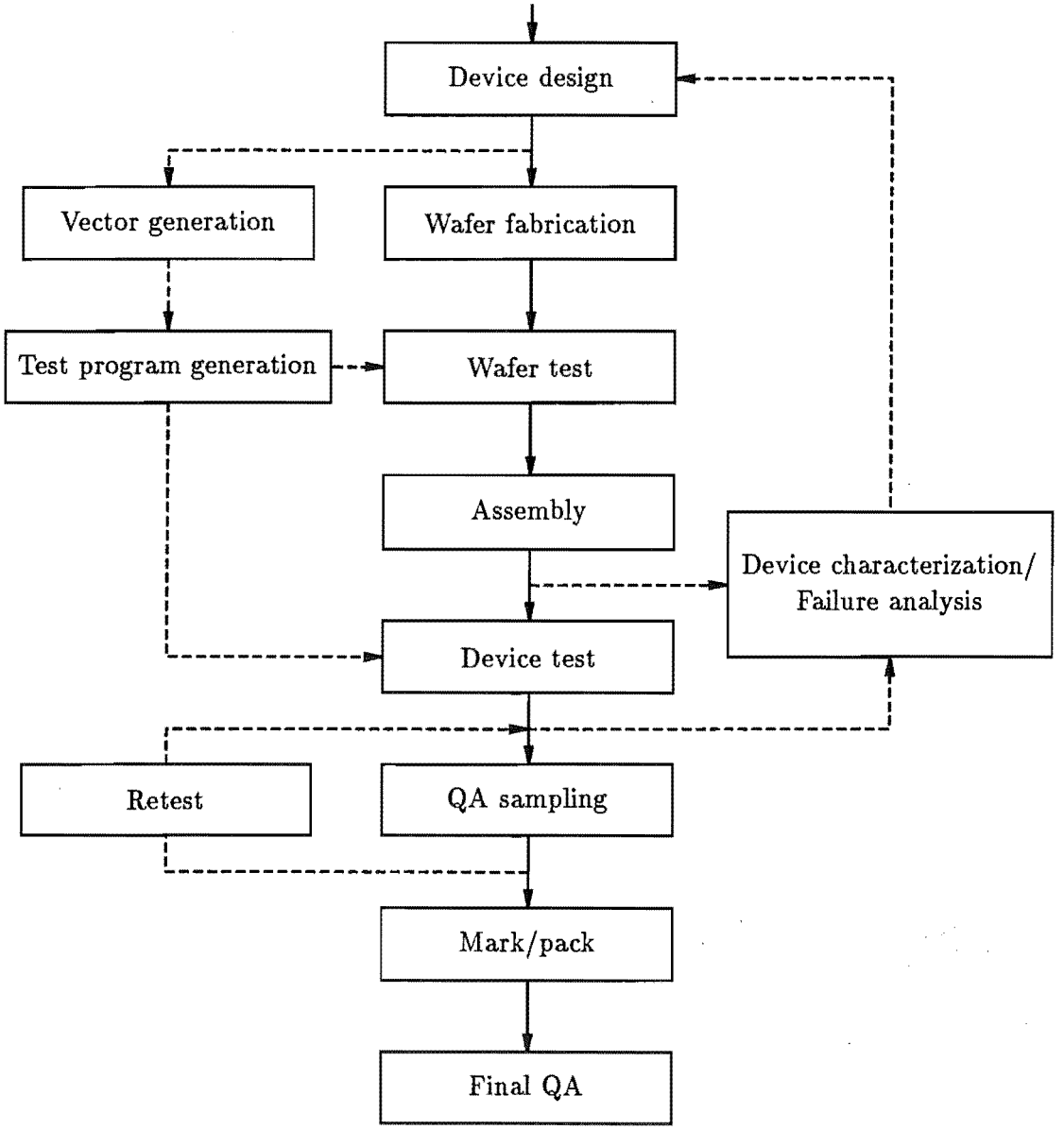


Figure 1.3 Flow chart of IC manufacturing (solid line) and test (dashed line) processes.

a verification of the design target specifications and the establishment of production specifications for the timing and parametrics of the devices.

To allow for the tester's inaccuracy, production testing is done to a tighter specification than the published user specification.

As a check on the production testing process, a quality assurance (QA) test is performed on a sample of the devices.

1.3 INTEGRATING DESIGN AND TEST

In the past, engineers designed a chip and *then* test engineers worried about testing it. Now, because of the complexity of VLSI circuits and the sheer number of specific application designs that are being generated, a designer must not only design the chip but also decide how to test it. Thus, testing must be considered from the very beginning.

1.3.1 Design for Testability

The definitions of testability are numerous; some are formal, others are informal. An informal definition of testability is as follows [BENNETS, 1982], "A design is testable if and only if a set of test patterns can be generated, evaluated, and applied in such a way as to satisfy pre-defined levels of performance, in terms of fault detection, fault location, and test application criteria, within a pre-defined budget and time scale".

The number of test patterns required to verify the operation and performance of a design increases exponentially with its complexity. Design for Testability (DFT) methods are employed to ensure that a design is testable. Some DFT techniques such as Level-Sensitive Scan Design (LSSD) reduce test pattern generation for sequential circuits to that for combinational circuits by enhancing the controllability and/or observability of all the memory elements. However, even for a combinational circuit, 100% test coverage of large-scale circuits is generally very difficult to achieve [MOTOHARA and FUJIWARA, 1984]. Without DFT rules, designs may be testable, but the probability of creating an inherently testable design decreases sharply with increasing circuit complexity [HNATEK, 1987].

1.3.2 Basic Requirements for a Testable Circuit

Testability analyses during the design of an ASIC are simple ways of measuring how easy it will be to test the circuit. The basic requirements of good design for testability are [KROEGER, 1984]:

- Controllability: the ability to set the state of internal nodes.
- Observability: the ability to observe the state of internal nodes.
- Partitioning: breaking the network into pieces to achieve a dramatic reduction in both test and simulation times. The philosophy is one of *divide and conquer.*

1.4 TEST DEFINITIONS AND METHODOLOGIES

There are various definitions and methods of testing. No matter how it is defined or performed, the common goal is to gain the greatest benefit while minimizing test and repair costs.

1.4.1 Definition of Test

A general definition of test is defined as "a procedure or action taken to determine under real or simulated conditions the capabilities, limitations, characteristics, effectiveness, reliability or suitability of a material, device, system, or method" [MIL STD 1309C, 1983].

The above definition implies that a number of different tests may be required to achieve the various goals, so demanding different techniques designed to verify the several aspects of that material, device, system, or method.

1.4.2 Test Methodologies

In IC testing, several identifiable techniques have been developed, as described below [STEVEN, 1986].

1.4.2.1 The testing purpose

Some commonly used techniques are

- Characterization
  The most extensive phase of testing is characterization and design verification or simply, *characterization* testing. During characterization, test time is less important. The main goal is to obtain the most accurate data for design-centring.
- Production
  The objective of production test is to insure that each device meets its specifications, and functions correctly while at the same time minimizing test time for maximum cost effectiveness.
- Burn-in
  Burn-in test is also refered to as *end-of-life* testing. The aim is to ensure that the device will function correctly for a specified period of time, and relates to device reliability.
- Incoming inspection
  System manufacturers must insure that all components to be used in their systems function according to their specification. They often test these devices by performing a QA test on a sample of their purchased volume.

1.4.2.2 Manufacturing level

The interface between the tester and the device depends on the manufacturing level of that device. This has a major effect on the electrical environment that the device is being tested in, and must be accounted for in the results. The principal tests are

- Wafer probe test
- Packaged test (or *electrical* test)

1.4.2.3 Test method

There are two kinds of test used in both production and verification testing:

- Functional testing
  Functional testing, or go/no-go testing, verifies that the device performs according to its truth table. The goal is to show that the device works. Functional testing, generally, can be performed by comparing the actual output from the device under test (DUT) and the expected data predicted by a simulator or a *known good* device.

- Parametric testing
  In the verification process, after completing functional testing, designers typically move on to parametric measurements which can be divided into two classes: AC and DC parametric testing. AC tests generally involve measuring setup and hold times, propagation delays and maximum operating speed. DC parametric measurement involves input current, output voltage levels, output current or drive capability of the device, and noise margins of both high and low logic levels. There are two modes of measurement in DC parametric testing, force current/measure voltage, and force voltage/measure current. Through such measurements, designers make independent evaluations of a foundry's fabrication process or obtain an insight into device performance margins.

1.5 DEVICES AND THEIR PACKAGING TECHNOLOGIES

Test techniques and specifications required to test an IC also depend upon the process technology of the DUT and its packaging. In this research, both the device and its package are included in the analysis as part of the load of the transmission path between the tester and DUT. In this initial study, the DUT is considered as a load on the transmission path without specifying any particular DUT family. However, this research has as its first goal a CMOS tester.

The discussion presented in this section may not exactly reflect the present status of ASIC technologies since they are rapidly changing and are outside the scope of this thesis, but newly developed and advanced technologies such as submicron Si, GaAs and other III/V materials, and BiCMOS devices are implicitly included.

1.5.1 Device Technologies

There is no one supreme technology. The choice for a specific application may be made on the basis of performance, availability and cost. Therefore the tester must be capable of addressing the major commercial technologies.

Bipolar and MOS technologies support the major semicustom and full custom logic families. Common to all bipolar families, TTL, I^2L, ECL and others, is the bipolar

junction transistor (BJT) operating either in a saturating switching mode, or in faster circuit configurations in a non saturating mode. The field-effect transistor (FET) is the major active device in the current MOS technologies, NMOS and CMOS.

1.5.1.1 Comparison between DUT technologies

A comparison of different logic families can be done in various ways. One of the commonly used methods is to compare them in terms of delay-power product. Figure 1.4 compares these major logic families [MURRAY and REEKIE, 1987].

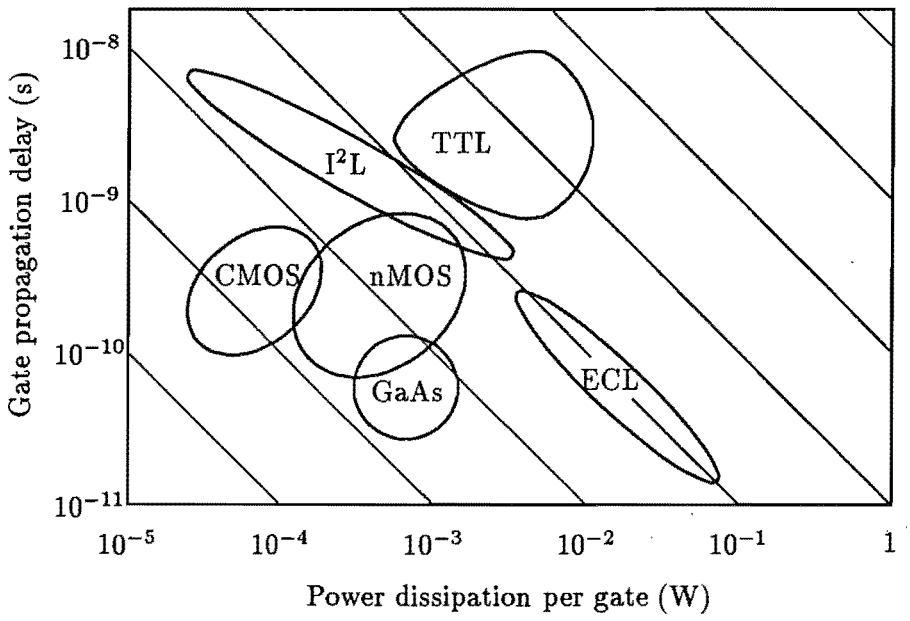


Figure 1.4 Delay-power products of different logic families.

1.5.1.2 IC power dissipation vs frequency

The power dissipation per gate of the CMOS family depends on load capacitance, power supply voltage and operating frequency. Power dissipation is expressed as $P_d \propto C_L V_{DD}^2 f$, where C_L is the total capacitance, V_{DD} is the supply voltage, and f is the clock frequency. Figure 1.5 [MUROGA, 1982] shows the relative speed/dissipation behavior of CMOS and several bipolar logic families and demonstrates that CMOS dissipation is strictly proportional to switching frequency. All other families, including NMOS, show a constant dissipation below some critical frequency. Above this frequency significant extra dissipation proportional to frequency results from circuit capacitances charging and discharging through the switching transistors.

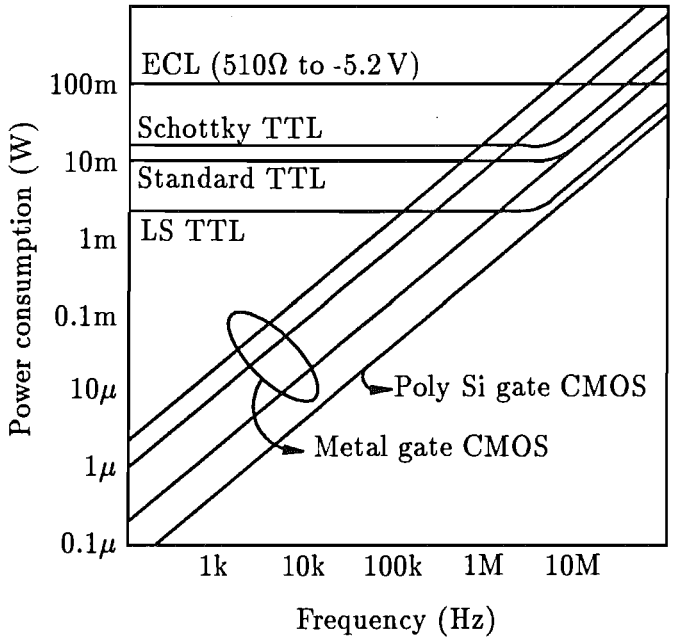


Figure 1.5 Power consumption of Isoplanar CMOS and various bipolar logic families at different frequencies.

1.5.2 DUT Packaging Technologies

The designer who leaves the world of standard products and moves into ASIC design is not only responsible for developing the correct test pattern but also specifying the correct package for his chip. Improved semiconductor manufacturing technology leads to high complexity, high density and high speed in ASICs. The use of VLSI devices creates packaging problems in two major areas.

1. High speed signal propagation
2. High package interconnection density

1.5.2.1 Requirements for ASIC packages

A package, as the semiconductor industry defines it [JOHNSON and LIPMAN, 1986], "is the material around the silicon chip that acts as physical protection and an interconnection between the chip and its functional environment". The ASIC package has many requirements, most of which are common to all semiconductor packages. These include:

- Physical support and protection
- Thermal dissipation
- Electrical interface

The package and interconnection technique must not significantly degrade the chip performance and should also provide:

- Easy and reliable attachment of the package to the system
- Easy repair technique
- Low tooling cost to attach and remove devices
- Low volume and low mass

1.5.2.2 Package hierachy

Figure 1.6 shows system levels in ASIC packaging. The first level of connection is the connection of the chip itself to the substrate in the case of a multichip module or to the chip package in case of a single chip module. This can be done by one of three ways; wire bonding, tape-automated bonding (TAB), or controlled collapse bonding (flip chip) [BAKOGLU, 1990]. Beam leads, which consists of thickened metallisations protruding beyond the chip, will not be included in this discussion. They have been used by AT&T Bell laboratories and Hewlett Packard but the process has not gained a wide commercial acceptance [HASKARD *et al.*, 1982].

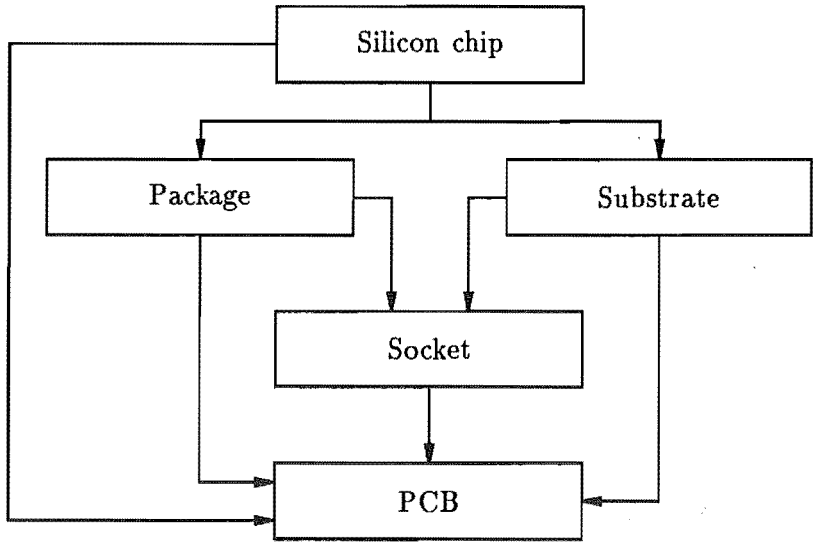


Figure 1.6 Levels of ASIC packaging.

Wire bonding is widely used for connection either within a package or directly to the substrate. The irregular structure of bonding wires makes accurate calculation of their electrical parameters difficult. The typically large parasitic inductance of bonding wires (approximately 2–5 nH) is a major problem [BAKOGLU, 1990].

Tape-automated bonding systems are commonly used in large production runs. Low manufacturing costs and high product reliability are characteristic of TAB systems

especially for VLSI where high I/O density and high speed electrical performance are necessary.

The IBM flip chip is another alternative whereby the chip is glassed over, etched for contact windows and solder balls formed in these holes. The balls can be placed either on the chip, termed *bumps on the chip*; or on the substrate, termed *bumps on the substrate*. Those methods minimize the length of the electrical connections between the chip and the substrate and introduce less parasitic inductance and capacitance. However, visual inspection of such solder bonds is difficult and frequently impossible because they are hidden between the chip and the substrate.

Figure 1.7 illustrates these methods for the first level of connection, while Table 1.1 describes some electrical properties of these interconnection methods [PEDDER, 1989].

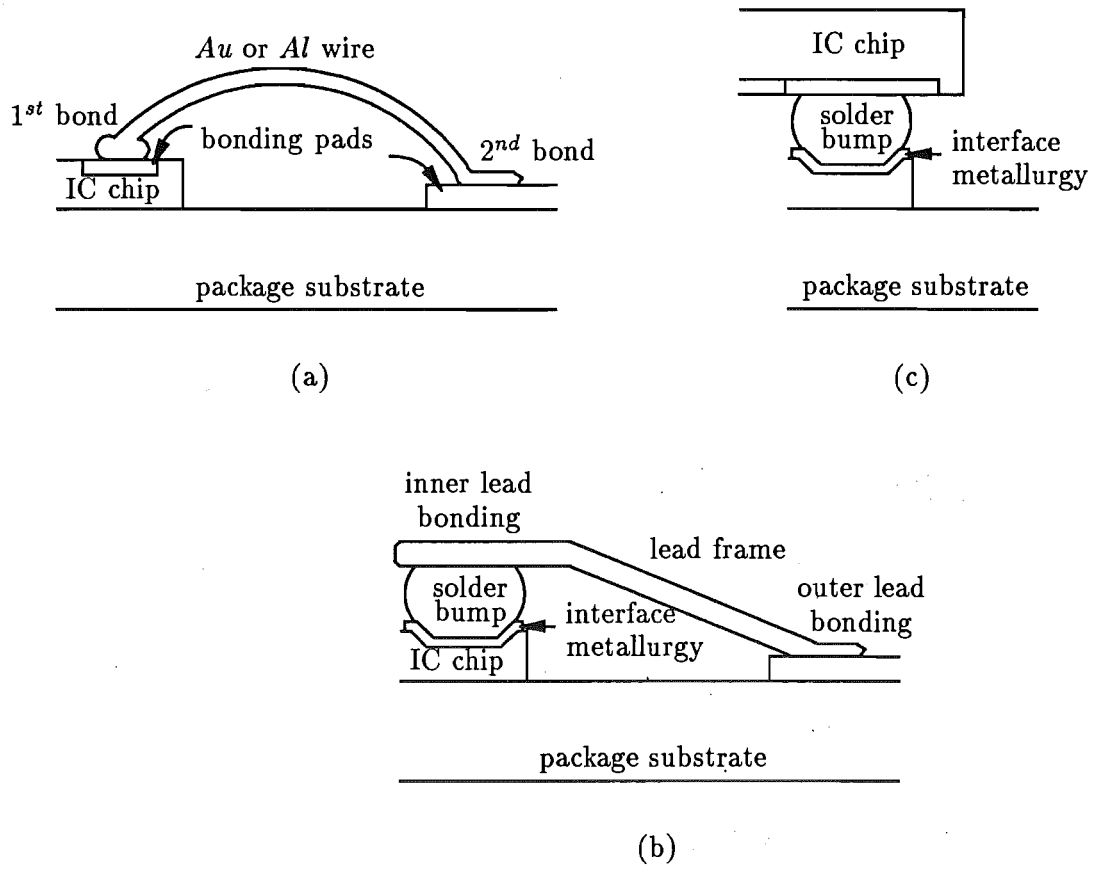


Figure 1.7 First level connection (a) wire bonding (b) tape-automated bonding (c) flip chip.

For the purpose of testing or evaluating the performance of a prototype chip, wire bonding is the most suitable. When this chip has passed into the production line, its packaging might be changed to enhance the production throughput. Understanding the hierarchical-structure of device packaging is very important, especially during device characterization. The test engineer must account for the effects of a package on the measured values to obtain the actual device performance.

	Wire bond		TAB	Flip chip
Material(s)	*Al*	*Au*	*Cu*	*Pb/Sn*
Bond geometry	25 μm diameter		25×100 μm tape	125 μm diameter
Typical pitch	170 μm perimeter		200 μm perimeter	250 μm area
Bond resistance	142 mΩ	122 mΩ	17 mΩ	1.2 mΩ
Interbond capacitance	0.025 pF	0.025 pF	0.006 pF	< 0.001 pF
Bond inductance	2.6 nH	2.6 nH	2.1 nH	< 0.2 nH
No. of I/O per chip				
4 mm chip size	92	92	80	256
8 mm chip size	184	184	160	1024

Table 1.1 Some typical properties of chip bonds.

There are many different packages available for surface mount and through-board assembly. Each involves some electrical and/or mechanical trade off. Figure 1.8 shows some of the available types of package.

In the design verification process one of these packages is selected to hold the prototype chip on the DUT interface board. The criteria for selecting a package depend on operating speed, I/O channels, power dissipation, and the economics of using that package. Obviously, it is inappropriate to put a 144 I/O channel chip into a low-cost plastic dual-in-line package (DIP). Chip carrier and pin-grid array packages using either military-hermetic (ceramic) or commercial-plastic (PCB) substrates, are needed for such high pin-count chips. For high speed devices, multilayer PCB substrates provide better electrical performance. Their copper traces offer lower resistance and inductance, and the dielectric constant is approximately half that of alumina ceramic. The PCB package cost is, typically, less than one third that of the ceramic version [BLACKSHAW and DANCE, 1986].

The next level of connection is that from the package to a chip socket or the circuit board (Figure 1.6). The two major connection techniques are through-board and surface mount. In both cases, the device can either be socketed or attached directly to the board.

1.5.2.3 Design for testability at board level

With the complexity of VLSI devices and as little as 25 *mil* bonding pad pitch in surface mount technology (SMT), today's circuit board designs are becoming very difficult to inspect visually for assembly defects. The effort put into the design for testability of ASIC would be meaningless if DFT is not further considered at board level.

Built-In Self-Test and Boundary Scan are two of the most promising solutions for

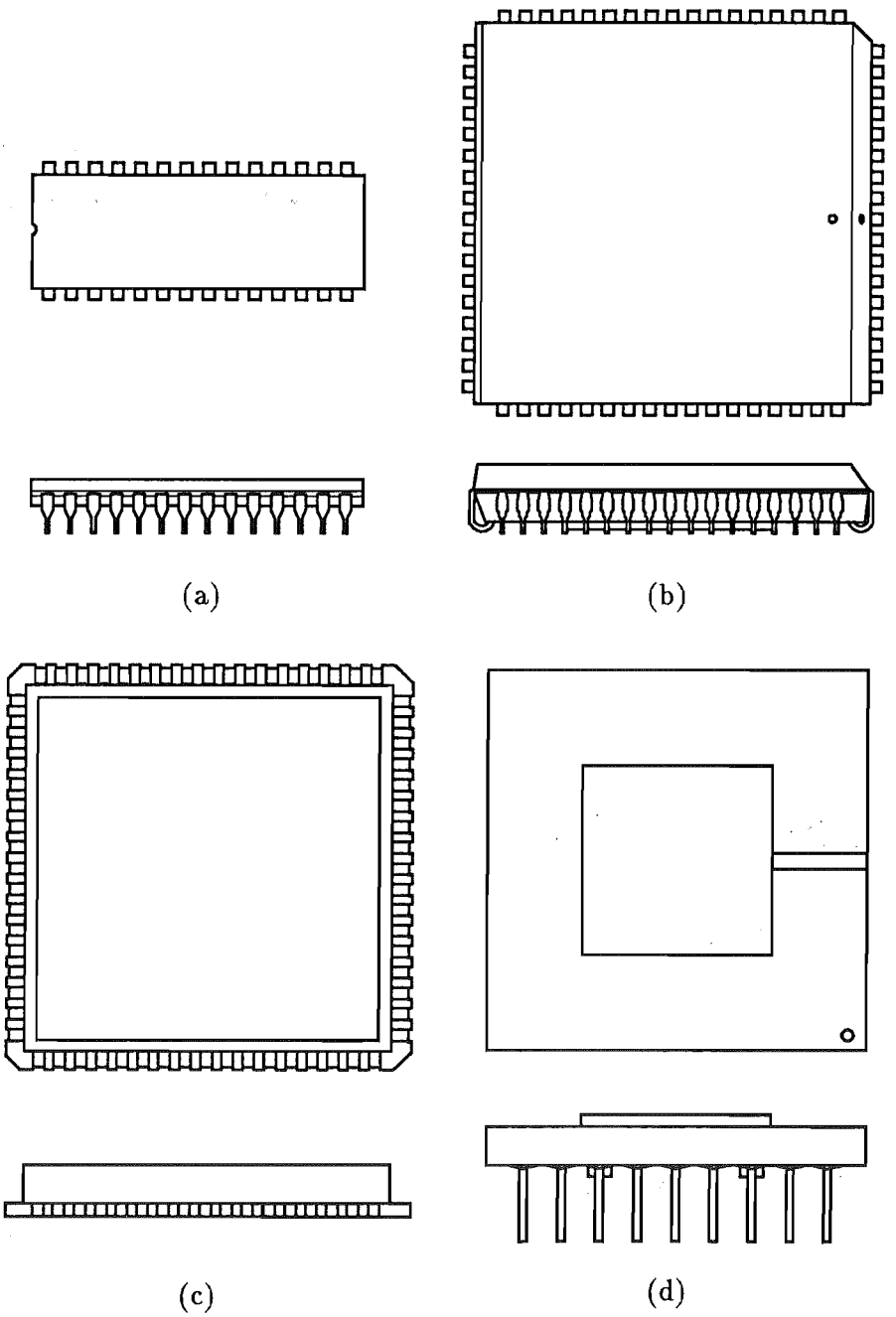


Figure 1.8 Several types of IC package (a) Dual In-line Package (DIP) (b) Plastic J-Leaded Chip Carrier (PLCC) (c) Leadless Ceramic Chip Carrier (LLCCC) (d) Pin-Grid Array (PGA).

board level testing. BIST is a design with inclusion of on-chip circuitry for testing. Such circuitry is responsible for test generation, test application and response evaluation. Since self-test circuitry uses some chip area, the chip's yield, performance, and reliability will be affected.

The boundary scan concept allows one to access and control all the primary input and output pins on the chip or PCB from outside [HASSAN *et al.*, 1988]. The Boundary Scan proposal was originally developed by the Joint Test Action Group (JTAG) and is now described by the proposed IEEE standard P1149.1. Devices incorporating the proposed boundary scan architecture offer significant advantages particularly when testing prototyte systems [HALLIDAY *et al.*, 1989; BALLEW and STREB, 1989].

CHAPTER 2

ASIC TEST AND VERIFICATION SYSTEM

This chapter describes the evolution and basic structure of automatic IC test systems. Test equipment and test head architectures currently employed in VLSI testers are discussed in section 2.1. A discussion on the interface between the tester and the host computer, and the tester and the DUT is presented in section 2.2. Emphasis will be on tester-DUT interface problems, where this research is directed.

Section 2.3 introduces some signal propagation concepts in a high speed digital system. Section 2.4 outlines the general requirements and specification for an ASIC tester.

2.1 THE AUTOMATIC TEST SYSTEM

IC test systems may be grouped into three classes; benchtop, dedicated, and general purpose [HEALY, 1981]. Benchtop testers usually have limited test capability and are small in size. The dedicated tester is specialized for one device family such as memory. The salient feature of the general purpose tester is a flexible configuration to accommodate almost any device type. Sophisticated computer-controlled test hardware and software is mandatory. The following discussion deals only with general purpose ATE.

The basic components of any general purpose automatic test system include a computer or controller, a test head, a tester-controller interface, and a tester-DUT interface. Figure 2.1 illustrates the basic components of a general purpose IC tester.

Details of the controller and tester-controller interface will not be further considered.

2.1.1 Evolution of IC Automatic Test Systems

The first commercially available automatic IC tester, the Model 4000, was developed by Fairchild in 1964. It consisted of various constant current and voltage sources and a measuring unit. It was programmed from a magnetic disc with a fixed word format, in machine language, and it had the ability to *burst* a series of digital pulses to test the functionality [HEALY, 1981].

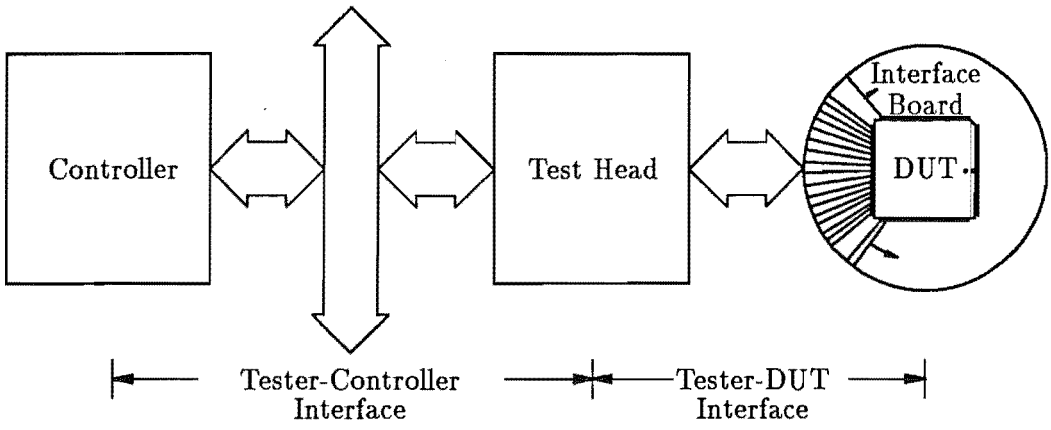


Figure 2.1 Basic components of a general purpose IC tester.

The next commercial tester on the market was the Model 553, manufactured by Texas Instruments. Similar in concept to the Fairchild Model 4000, it was programmed with a continuous paper tape. Teradyne introduced the Model 259, the first tester controlled by a digital computer, in 1967 and opened a new era of semiconductor ATE.

The need for a high speed, accurate, multipin tester was recognized in 1976 in a feasibility study completed by a leading semiconductor research organization [SUDO, 1979; KAZAMAKI, 1985]. The Takeda Riken Advantest T3380, a 100 MHz, ±500 ps timing accuracy, 384 pins split I/O tester, was developed in 1976 and established new levels of accuracy and performance in VLSI test systems [KAZAMAKI, 1985].

Megatest Inc. introduced the Mega One, the first tester based on Tester-Per-Pin (TPP) architecture, in 1983. By utilizing individual signal paths, the TPP approach eliminates a number of error sources and allows the magnitude of all errors to be closely controlled through an automatic calibration process [CATALANO *et al.*, 1983].

Since the beginning of the VLSI era, the speed and performances of IC test systems have been improved to try and keep up with the complexity and speed of these new devices. The 250 MHz Advanced Test System (IBM) [CHANG *et al.*, 1987] and the Ultimate 500 MHz (NTT) [TAMAMA *et al.*, 1988] have been reported to the International Test Conference 1987 and 1988 respectively. However, these are multimillion dollar systems and they are not available commercially.

2.1.2 Available Test Equipment

The decision whether to commit an ASIC design to production lays a heavy responsibility on the designer, who must thoroughly evaluate the ASIC prototype supplied from a foundry. He has the choice of assembling his own test system using pulse or data generators, oscilloscopes, counters and logic analyzers, or to use a production IC tester. A self-built test setup or rack-and-stack instrumentation does not offer solutions such as high channel count, pattern-edit-programmability or overall specified system

accuracy. Hence the self-built setup is seldom very effective. A production IC tester is more complete but also more expensive. The cost ranges from US$40,000 for an IC Design Verification System up to US$2 million for a state-of-the-art VLSI Test System[1]. A wide variety of performance levels is available. Test rates are running as high as 750 MHz, pin-count of more than 512 pins, memory depth up to 1 Mbit/channel, edge-placement resolution as fine as 10 ps, and overall system timing error down to ±20 ps. However, there is no single system that combines all these performance levels.

Tester functionality with high accuracy and resolution cannot be met with general purpose tools and not every design department can afford a $2 million tester. There is a need for a verification tester that offers test and development capabilities at an affordable price yet contains significant test functionality. Prototype testers are ideal for ASIC prototype evaluations, because of the short design cycles and the potentially inexpensive testing requirements of these ICs. Table 2.1 lists representative ASIC prototype verification testers.

2.1.3 Tester Architecture

The structure of the test head for VLSI testers needs to be improved because of increasing speed, performance, complexity and pin-count of the IC under test. The quest for improved timing accuracy in high pin-count VLSI testers has altered the basic architecture of the test system itself. Traditionally, testers have revolved around a Shared-Resource architecture in which a small number of central timing resources are distributed through a large switch matrix to groups of device pins. This arrangement leads to a complex timing path between master clock and DUT pins. One way to simplify the timing chain is to place a timing generator behind each tester pin, known as a Tester-Per-Pin (TPP) architecture.

Figure 2.2 shows block diagrams of the TPP architecture and the Shared-Resources architecture [BIERMAN, 1984; McMINN, 1985].

With the increasing cost of VLSI testers, maximizing utilization of tester resources has become important. A test site must purchase a tester that can handle the highest pin-count device that will ever be tested. In practice, only a small number of high pin-count devices and a larger number of lower pin count will be tested resulting in a significant portion of the tester resources sitting idle much of the time. A reconfigurable resource architecture [EDWARD, 1984; O'KEEFE, 1989], which can be reconfigured from one high pin-count test head to multiple independent lower pin-count test heads, provides improved hardware utilization.

2.1.4 The Test Head

To produce a tester with adequate performance at an affordable price, careful consideration of the user's testing requirements and attributes of the DUT technologies must be

[1]These prices were quoted during 1987–1988, and they are not meant to be accurate.

Manufacturer	Model	Maximum pin-count	Vector depth (kvectors)	Test rate (MHz)	Edge-placement resolution	Real-time comparison
Cadic Inc.	STM5100	256	64	10	1 ns	Yes
	STM5200	256	64	20	1 ns	Yes
Hewlett-Packard Co.	HP81810S	256	16	50	100 ps	Yes
Hilevel Tech. Inc.	TOPAZ I	288	64	25	500 ps	Yes
	TOPAZ II	288	16	50	500 ps	Yes
	TOPAZ V	320	16	110	500 ps	Yes
Tectronix Inc.	DAS9260	135	8	50	1 ns	No
	DAS9262	203	8	50	1 ns	No
	DAS9264	271	8	50	1 ns	No
	LT-1000	256	256	50	200 ps	No
Integrated Measurement System Inc.	Logic Master HS (General purpose)	384	16	20	100 ps	Yes
	Logic Master HS (High pin-count)	512	16	20	100 ps	Yes
	Logic Master HS (High speed)	384	16	40	100 ps	Yes
	Logic Master ST	224	4	20	1 ns	Yes
	Logic Master XL	224	-	100	100 ps	Yes

Table 2.1 ASIC prototype verification testers.

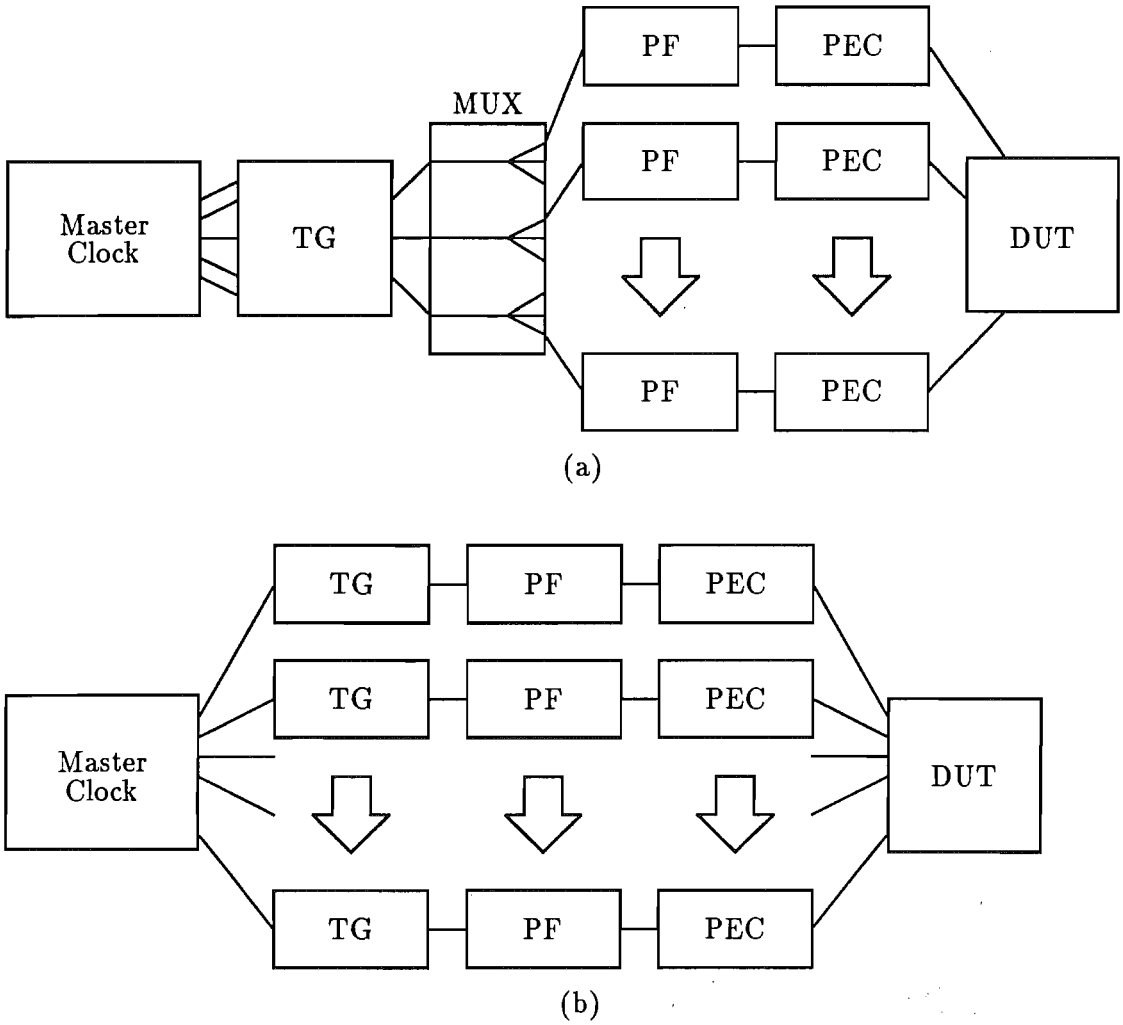


Figure 2.2 Tester architectures (a) Shared-Resources architecture (b) Tester-Per-Pin architecture. TG = Timing Generator, PF = Pin Formatter, MUX = Multiplexer, PEC = Pin Electronic Card, and DUT = Device Under Test.

made during the design process. Test head requirements for different DUT technologies reflect differences in design and fabrication for these technologies. The requirements for testing commercially available logic families have been described [BRAY, 1986].

Test heads on the first LSI test systems, which appeared in the early 1970s, were relatively simple. Because of the low pin-count of devices to be tested, the printed circuit boards containing test system voltage drivers and measuring circuits could be placed within 10–15 cm of the device under test [BARBER and SATRE, 1987].

Due to the increase in device pin-count and operating speed, today's VLSI testers have test heads with quite long transmission lines leading from the tester electronics to the DUT. With current technology, there is no effective way to communicate

signals between the DUT and PEC without using some form of transmission line. An electro-optical sampling technique, having sensor capacitance less than 1 pF, has been demonstrated by Photon Dynamics, Inc. [Henley, 1988], while electron beam and laser technologies have been applied in the test head [Concina and Richardson, 1987; Henley, 1984], but these techniques are too expensive and cumbersome for a low cost prototype tester. Furthermore, multiple layer metallization is being used to ease interconnect routing on-chip, leading to difficulty for methods based on surface analysis techniques such as Scanning Electron Microscopy (SEM).

2.1.4.1 IC testing processes

IC testing processes involve three principal steps:

1. *Generating* the test patterns
   The goal is a set of input patterns which will exercise the DUT under different modes of operation while trying to detect any existing fault. A test pattern, or *test vector*, describes a logical input sequence and an expected response. There are 4 accepted methods of generating a test vector, namely:

   (a) Manual

   (b) Algorithmic

   (c) Random

   (d) Simulation-aided

2. *Applying* the test patterns
   There are two ways to accomplish this step. The first is *external testing* ; the use of test equipment to apply the test patterns externally. The second is *internal testing*; the application of test patterns internally by causing the DUT to execute a self-testing procedure.

3. *Evaluating* the responses obtained from the DUT
   The major goal of this step is the detection of an erroneous response. A subsidiary goal is the location of a fault for diagnostic purpose. IC testers use two methods to evaluate the DUT responses.

   (a) Stored response
   In stored response testing, expected or good responses are stored in local memory of the tester and are used to compare with the DUT responses. The expected responses are commonly obtained as a partial product from the simulator.

   (b) Golden device (a *known good* device)
   Another way to evaluate the response of the DUT is to apply the test vectors simultaneously to both the DUT and a golden device and to compare their

responses to detect any faulty responses. Alternatively the responses of the golden device are stored and represent a known good response. The trick lies in identifying your golden device and verifying its continued goodness!

2.1.4.2 The elements of a test head

A test head contains electronic circuits that function according to the 3 steps described above. A typical block diagram of a present day test head is shown in Figure 2.3 [McMINN, 1985].

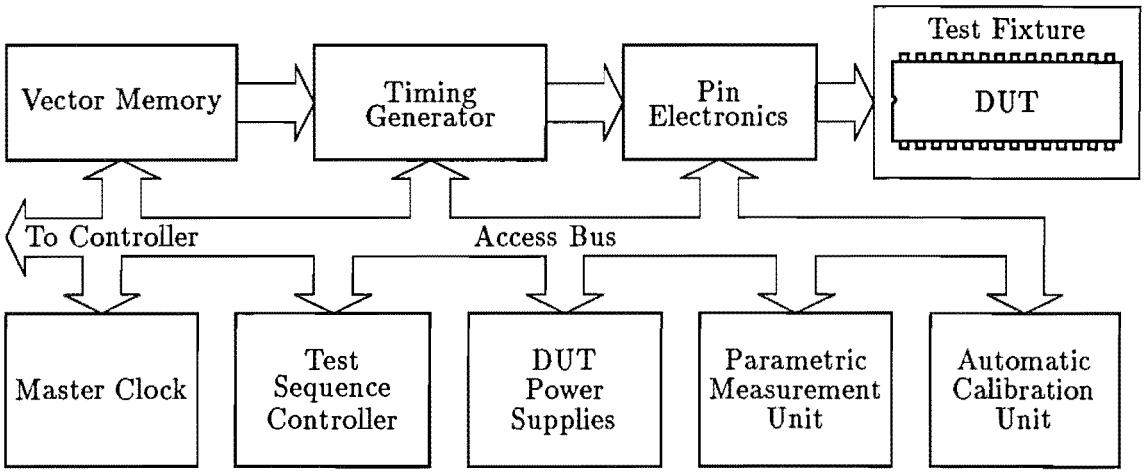


Figure 2.3 A typical block diagram of a test head.

In a test head, a vector memory is used to store test patterns. It provides stimulus timing, formatting, and driving through a circuit board called a Pin Electronic Card (PEC). A comparator or receiver, which is used to evaluate the DUT response, is typically included on the PEC.

Most new testers provide programmable current load circuits that will actively load the DUT outputs so that proper operation can be tested at the limits of the DUT rated loading. They also supply parametric test units or a parametric measurement capability.

A tester PEC communicates with the DUT through a test fixture. A good test fixture must provide both electrical and mechanical interfaces between the tester and the DUT. Stimuli should be transmitted and received accurately without degradation. Unfortunately, there is no such ideal test fixture available today.

An automatic calibration unit is used to account for the imperfection of the test head. This topic will be discussed in detail in the next chapter.

2.2 TESTING INTERFACE

Generally in a test system (Figure 2.1) there are two interfaces, one between the computer or controller and the test system, the other between the DUT and the test head. The first interface is for transfering test vectors from a controller to the test system and receiving results from the test system to analyze, interpret and display. The second is for passing signals between the test head and the DUT. Only the second interface will be discussed in detail.

2.2.1 DUT-Test System Interface

TPP architectures employ PECs which stimulate the DUT and sense its response. Present-day technology requires that controlled-impedance transmission lines connect the PECs to each DUT pin.

Each PEC interfaces with the DUT through a transmission line, as shown in Figure 2.4 which represents a typical test environment of a modern high speed VLSI tester. The PEC is bidirectional, with a *Driving* mode when the DUT is driven by the tester and a *Receiving* mode when the PEC is to receive signals from the DUT. Fast-edged waveforms stimulate reflections at unavoidable transmission path impedance discontinuities.

Each PEC–DUT path and load must differ somewhat from the others because no test fixture can have identical pathlengths to all pins and there is no effective constraint on the DUT loading.

2.2.1.1 Driving the DUT

The reverse-terminated PEC launches an approximately half-amplitude pulse toward the DUT where, because the DUT input impedance is (typically) much higher than the line impedance, it nearly doubles its amplitude. The pulse-shape at the DUT differs from that at the PEC output because the imperfect transmission line exhibits nonlinear frequency dependent amplitude and phase response. The reflected wave is nearly absorbed at the PEC reverse termination, but C_{PEC} causes a small reflection back to the DUT, delayed by the round trip time.

State-of-the-art PECs achieve high speed by employing a fully integrated PEC on a state-of-the-art CMOS chip, or else use ECL or even GaAs technology. Such a Pin Driver can stimulate the DUT with signals having transition times < 1 ns.

Preferably, the PEC should drive a short line to a very low capacitance test fixture, but such ultra-compact structures lead to severe crosstalk and cooling problems. Cox [1987] shows that such ultra-compact structures are unnecessary, provided that *electrically known* high quality lines are used.

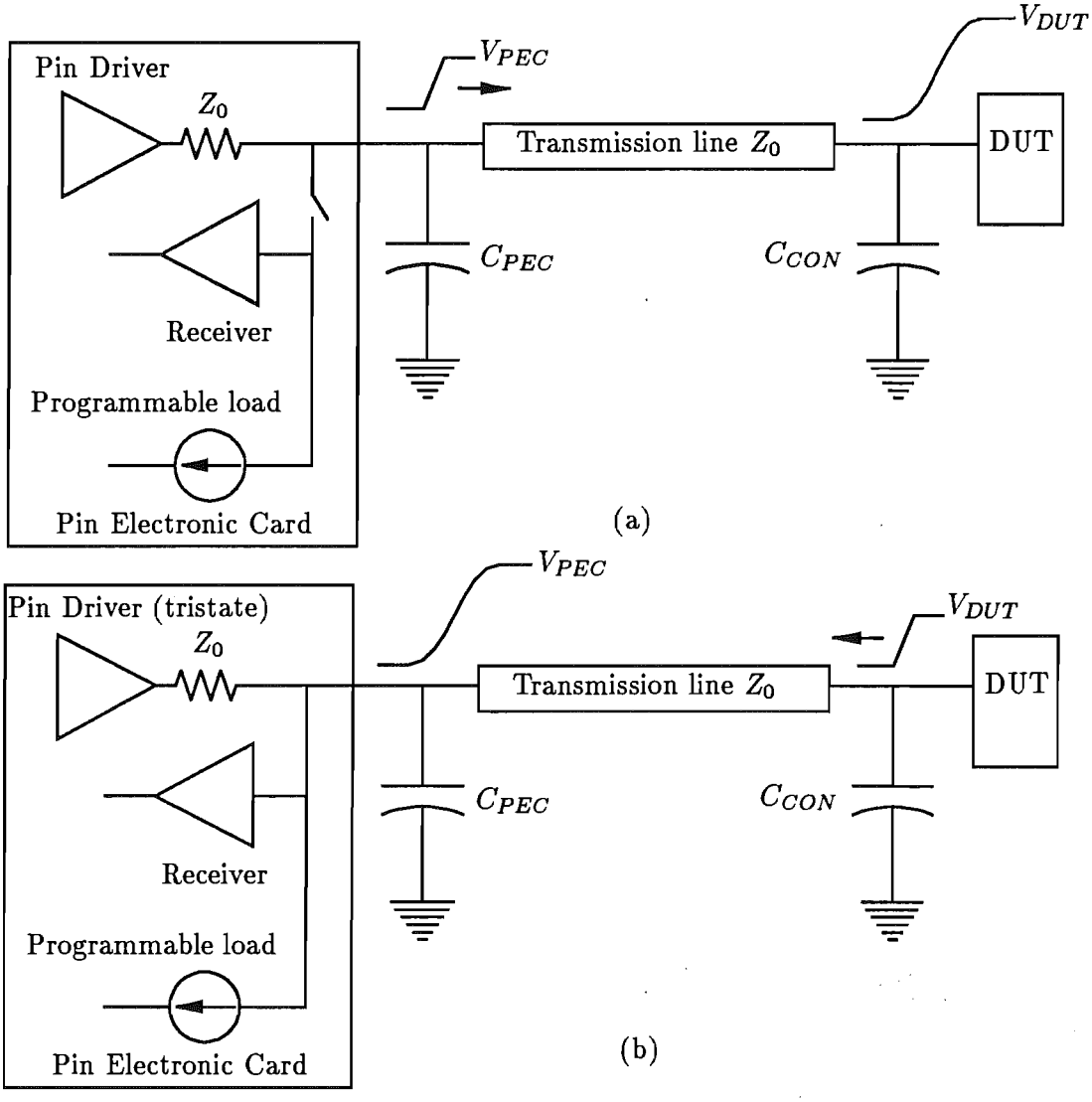


Figure 2.4 Bi-directional PEC–DUT Interface (one channel) (a) driving mode (b) receiving mode.

2.2.1.2 Sensing DUT output

When a PEC receives a signal from a DUT output, a reflection back to the DUT could be very serious because MOS and TTL driver output impedances seldom match the transmission line, causing a significant second reflection back to the PEC. The first reflection could be eliminated by matching the PEC receiver to the line. That suits ECL, but could lead to excessive power dissipation in MOS and TTL devices.

DUT output resistance, generally different in the logic high and low states, influences the waveform received by the PEC [PETRICH, 1986]. Input/Output structures and test head requirements for major DUT technologies are described by BRAY [1986].

DUT waveforms incident on the PEC receiver differ, for the same reasons as above,

from the actual waveforms at the DUT output pads. Correction to the measured waveforms might be through either a correction table or direct mathematical calculation.

Impedance mismatch between the DUT output and the signal path can be serious for a DUT with fast transition time and low output resistance, causing multiple reflections (ringing) in the transmission path. Cox [1987] specifies a series resistor between the output pad of such fast edge devices and the test head transmission line to achieve an approximate impedance match to the line. Instead of a series resistor a miniature unity gain buffer amplifier, fabricated in Thickfilm technology is proposed, to be placed close to the DUT to drive and backmatch the transmission line; an approach first suggested by BARBER [1984].

2.3 TRANSMISSION PATH CONSIDERATIONS

As the speed of the DUT increases, understanding the operation of a transmission line used in conjunction with high speed devices is necessary in order to completely characterize system operation. In the past, high speed circuitry has generally been in the microwave area of electronic systems such as a Microwave Integrated Circuit (MIC) chip. In contrast, digital logic system engineers have been working in the medium frequency (MF) band and low-megahertz or high frequency (HF) band. The ASIC revolution has involved both analog and digital circuit design, with speed up to the very high frequency (VHF) range. This has a severe impact on chip interconnection, packaging, printed circuit board design, system interconnection and test equipment.

2.3.1 Transmission Lines in High Speed Digital Systems

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) defines a *transmission line* as signal-carrying electrical circuitry, composed of conductors and dielectric material with controlled electrical characteristics, that is used for the transmission of high frequency or narrow-pulse type signals [STALEY, 1985].

2.3.1.1 When to use transmission line analysis ?

A long line is defined as having a propagation delay longer than half the transition time of the driving circuit. In the long line case, the reflection from the PEC will not significantly interfere with the waveform transition at the DUT. A transmission line can appear to be short or long depending on the waveform transition time. If, as is usual, the transition is exponential, the rise time (10%–90%) relates to the system bandwidth (f_h) as $t_r\,(\text{ns}) = 0.35/f_h\,(\text{GHz})$. Reflections cause small effects for a short line case because the edge rate is relatively slow and the high frequency energy content is smaller than for the long line case. The long line case is most likely for a high speed VLSI test and verification system.

Controlled-impedance transmission line techniques are necessary when the line length is long with respect to the wavelength of the highest frequency present in the

transmitted pulse, but if the transition time is greater than twice the propagation delay of the line, the connection path may usually be approximated by a lumped circuit.

2.3.1.2 Parameters for high speed performance

The major parameters in high speed signal propagation are:

- Signal transition time or signal rise time
  In this thesis, signal transition time is used when the signal is assumed to be an ideal ramp signal and signal rise time is used when the signal is not an ideal ramp signal. For an ideal ramp signal, rise time = 0.8 transition time.
- Propagation delay
- Crosstalk and line losses
- System bandwidth

Transmission line techniques for interconnection paths in high speed systems are often used to minimize waveform distortion and signal reflections from discontinuities.

2.4 TESTER SPECIFICATIONS

Integrated Circuits are moving toward increased complexity and mixed-signal circuits which employ a mixture of digital and analog techniques. To avoid increasing test time and cost, ASIC test systems must combine a variety of features within a flexible and easily operated test environment.

The operating rate of a gate is defined as the inverse of the gate delay and gives an idea of the speed at which the device is capable of operating, although the ASIC's speed will generally be much slower than that of a single gate. Therefore, the tester must not only operate at high speed, but must have good timing resolution and accuracy.

The major justification for increased accuracy in ATE is to increase product yield by reducing the go/no-go guardband widths. The more accurate the test the fewer the test uncertainties. The fewer errors made by ATE, the smaller the testing guardbands which means fewer good devices will be mistakenly rejected.

Another benefit of increased accuracy is the early detection of any variation in process control values that would adversely affect future product quality. The device designer needs to accurately determine the device's operating range during the characterization test. The customer needs reassurance that the device specifications are being met.

2.4.1 Test Parameters for Digital Circuit Characterization

Digital circuits range from simple logic gates through complex semicustom to full custom ASICs. Irrespective of their application and complexity, all digital circuit blocks can be characterized by their logic functionality and their input and output parameters.

A test system should provide stimuli with variable timing and levels, for both driving and receiving circuits, so that all AC timing parameters and DC parameters may be measured, including those of mixed-signal (analog/digital) circuits. A high resolution comparator on the PEC ensures reliable comparison of small time intervals and voltages. The following capabilities are essential for a VLSI tester.

2.4.1.1 Speed

A major factor in the real environment is the operational speed. Speed is being used as the most important selling feature in recent test and verification system market entries [BARIL, 1986]. The tester data rate must be fast enough to realistically exercise the device being investigated. As the test speed is increased, the bandwidth of the tester-DUT interface must increase to accommodate the higher data rate. For most verification tasks, faster is not necessarily better. Increasing the speed of a test system significantly increases PEC power demand and the cost of the system hardware. This cost increase illustrates the type of trade-off that designing for speed alone requires: the system price must be increased or other features must be sacrificed. The ATE purchaser will decide whether the parts to be tested justify the greater expense.

2.4.1.2 Timing parameters

For error-free operation, synchronous devices, such as RAM or latches, require that the applied data be stable for a *setup time* before, and a *hold time* after, the active clock transition. Asynchronous devices, such as simple logic gates, also require a specific response time during which the input data must be stable.

The propagation delay of a gate is the time between input stimulation and output reaction. The value depends on the complexity and technology of the circuit. Propagation delay, as well as setup and hold times are timing parameters that limit a circuit's data rate.

To measure setup and hold times, the stimulating instrument must deliver a functional pattern having appropriate timing parameters, represented by delay and width. The receiving instrument must recognize errors caused by these parameters being outside the required values. The values of these timing parameters vary from less than 1 ns for an ECL and GaAs logic family, to over 100 ns for a MOS logic family. Most testers measure these timing parameters by stepping the delay until the DUT fails. For this reason the timing resolution of the measurement instruments must be fine enough (typically in the order of a few tens of picoseconds), so an instrument with 1 or 2 ns timing resolution is quite inadequate.

Pulse rise and fall times are important because each DUT family exhibits a different response to different rise and fall times. To accurately measure DUT timing parameters, the rise and fall times must be set properly.

Both systematic and random timing errors occur so a measurement guardband, as shown in Figure 2.5, is used to provide the safety margin.

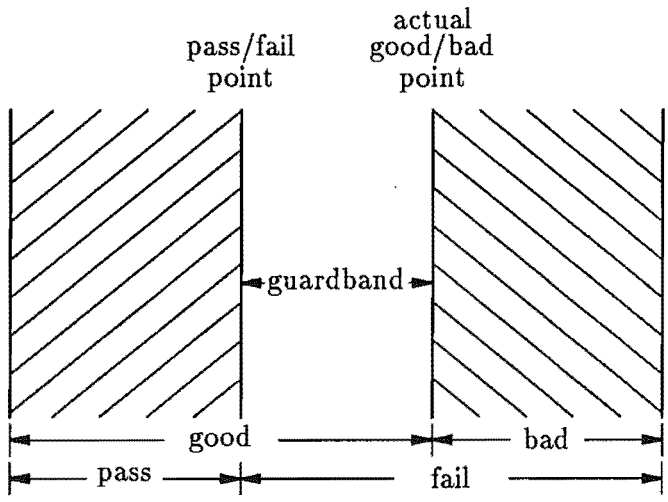


Figure 2.5 Guardband testing.

2.4.1.3 The level parameters

Other causes of malfunction are found in the voltage domain. Although the trend of standard power supply voltage for MOS devices is towards 3.3 V, TTL logic families use 5 V. PEC driver high voltage (V_{IH}), low voltage (V_{IL}), PEC receiver high voltage (V_{OH}) and low voltage (V_{OL}) are programmable and can be adjusted to cover major DUT families voltage swings (typically from -2 to +7 V with 10 mV/step) so that both input threshold voltage and output drive capability of the DUT can be verified. Such high-resolution programmable voltage levels are sufficient also to evaluate the small swings of a few hundred millivolts characteristic of ECL logic families.

2.4.1.4 The pattern format

While the timing and level parameters are alike for all digital devices in a given family, their logic functions are unique. These logic functions are usually expressed by a truth table which determines the bit patterns with which the DUT must be functionally tested.

To handle the complex timing requirements of ASICs, IC testers offer the designer a variety of data formats. Figure 2.6 shows some commonly used data formats.

2.4.1.5 Memory depth

This term is often refered to as the capacity of local memory available in the test head of an IC tester. Test vectors are loaded from the host controller into these memo-

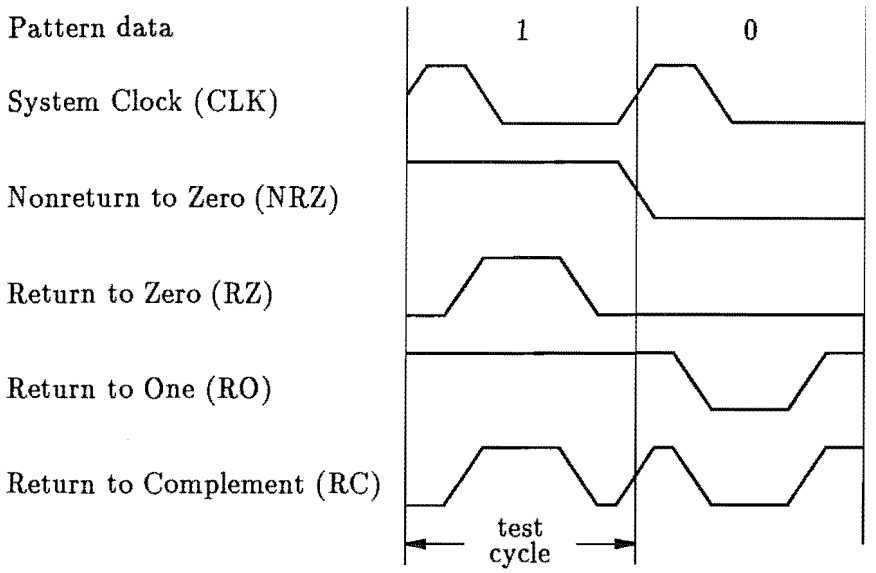


Figure 2.6 Some commonly used data formats.

ries. Therefore, large capacity memory is required to accomodate large vector sets and minimize vector loading time.

In production testing, the design is assumed to be correct and test vectors are used to screen out functional problems that may have been created by faulty processing. In a design verification system, the purpose is not to run a large number of vectors and obtain a yes/no decision as in production tester. The real benefit from ASIC verification systems is that the designer can put specific vectors into the chip to help determine the source of problems. Therefore, for verification testing, large memory capacity is not a major concern.

Most new generation ASIC verification systems have brought new ways to get more effective pattern depth that do not entail just putting more memory behind each pin [BARIL, 1986]. Most of these methods involve architectural changes to the test system. Adding loop counters and repeat vector counters permits compression of the vector files. Algorithmic pattern generation is another method of reducing the memory needed for each pin. This technique is primarily useful in testing memory and will become increasingly popular as more gate arrays have embedded RAM on the chip [BARIL, 1986].

2.5 SUMMARY

This chapter has described the basic structure and general requirements and specification for an ASIC tester. Building a complete low-cost ASIC test and verification system is the ultimate goal of this research. However, this work requires several man-years to complete. The initial work reported in this thesis is aimed at demonstrating an innova-

tive approach to improving timing accuracy and waveform quality in high speed ASIC testers. The proposed improvements are described in chapter 3.

The DUT-test system interface is investigated in detail to find a suitable model of a complete channel. A means of improving edge-placement accuracy and waveform quality, using a pre-compensation technique, is presented.

CHAPTER 3

THE PROPOSED IMPROVEMENTS

This chapter describes an innovative approach to improving timing accuracy and waveform quality in high speed, high performance IC testers. The approach is not aimed at replacing conventional calibration methods but rather at enhancing the accuracy and performance of such testers. This research investigates the effects of transmission path imperfection and the effects of the loads at both ends of the path. These effects have not adequately been taken into account in any conventional calibration methods known to the author.

Section 3.1 discusses the timing accuracy specification of modern IC testers and some conventional calibration techniques. The main objective of the proposed calibration method, described in section 3.2, is to compute a waveform that will compensate for path imperfections and loading effects and improve edge-placement accuracy and signal quality.

A comparison between Time Domain Reflectometry (TDR) and Frequency Domain Reflectometry (FDR) is presented in section 3.3. FDR is employed to measure both incident and reflected waves and therefore the voltage reflection coefficient (or S_{11}) of the loads at both ends of the transmission path.

Section 3.4 summarises the proposed system, and highlights the major parts detailed in this thesis.

3.1 TIMING ACCURACY IN MODERN IC TESTERS

Although the timing accuracy specifications of modern IC testers lie in the subnanosecond range, there remain timing errors of several nanoseconds, particularly when testing MOS devices [BARBER, 1983; 1984; PETRICH, 1986]. The sources of these errors can be placed in two categories; random noise and systematic errors [KEATING, 1987]. It has been shown that random noise error in a well-designed system is several orders of magnitude smaller than the accuracy specifications of today's testers [KEATING, 1986]. Therefore systematic errors are the limiting considerations. There are four major kinds of systematic timing error:

- Crosstalk
- Reflection due to impedance mismatch
- Bandwidth limitation
- Thermal effects

The first three are the dominant influences, associated with system interconnections, especially the interface between the test system and the device being tested.

Measurement errors and effects of the transmission path, and their tabular correction, have been studied by BARBER [1983] and PETRICH [1986], while analytical calculations of CMOS VLSI output pad voltages and currents were discussed by MOKARI-BOLHASSON and KANG [1988].

This research is based on the belief that errors occur principally at the interfaces between the PEC and DUT, and so the research effort is directed there. Thermal effects, which frequently cause timing errors in active devices, are not considered because they are of a different kind and can be independently dealt with.

3.1.1 Toward Standardization of ATE Timing Accuracy

Timing accuracy in an IC tester is a key factor in determining the quality of the verification process. As the DUT moves to higher and higher speeds, test systems must stimulate the DUT with faster edge and test rates. A general purpose VLSI test system with timing accuracy specification in the range of ± 1 ns or less is common. A standard to determine the timing accuracy of these testers has not yet been established. The specifications are defined in a rather *ad hoc* manner. A typical approach is to sum the errors from all possible sources as discussed by SUGAMORI [1981]. Although there is no formal agreement between ATE manufacturers on these specifications, they are widely accepted as a major indicator for comparing the performance of different testers. MYDILL [1987] has proposed a generic procedure for measuring and summarizing test system timing accuracy. In his paper, a definition of overall timing accuracy has been suggested, and will be discussed in section 3.1.3. He has also persuaded the industry to standardize timing accuracy specifications with focus on VLSI testers [MYDILL, 1988].

Eventually, standardization of timing accuracy specifications will ease comparison between testers from different manufacturers. Understanding and dissemination of the timing error information will thereby be improved.

3.1.2 Sources of Timing Error in VLSI Testers

Timing error sources may be classified in relation to the tester architecture. They are different from the error sources described previously, which are independent of tester architecture.

All the element blocks in a test head, such as those shown in Figure 2.3, are made programmable. Because the tester establishes all test conditions by programming, most timing errors are associated with such programmability [SUGAMORI, 1981].

The principal timing errors associated with each element, detailed analyses and procedures to minimize these errors are given by SUGAMORI [1981], in which the overall timing accuracy is defined as the sum of all these errors.

In this thesis timing error sources are considered under a broad classification, namely [MYDILL, 1987]:

- Test system error
- DUT insertion error
- Test fixturing error

The last two are independent of programming, and thus amenable to improvement described in this thesis.

Comprehending each of these timing error sources is important, because any of the three can have a significant impact on test results. A generic analysis of test system errors has been performed by MYDILL [1987] which did not, however, include DUT fixturing and insertion errors.

3.1.3 Definition of overall timing accuracy

A definition of overall timing accuracy (OTA) was presented at the 1987 International Test Conference [MYDILL, 1987], he later claimed that the definition and procedure received general support from tester manufacturers and members of the testing community [MYDILL, 1988]. The definition was presented in terms of tester functionality rather than a specific architecture or design. The key elements of his definition are:

- Comprehensive scope
- General applicability
- NBS (National Bureau of Standard) traceability

The definition is repeated here:

$$OTA \triangleq \pm(T_2 - T_1 - T_{ref}) \tag{3.1}$$

where

- T_1 is the programmed time of occurrence (relative to the start of any test cycle) of a specified point on either transition of a tester generated signal using:
  - any Pin Driver

  - any timing generator[1]
  - any delay
  - any amplitude
  - any signal format

- T_2 is the programmed time at which the point is detected by the tester using:
  - any pin receiver
  - any timing generator[1]
  - either comparator (expect "1" or "0")
  - window or edge compare

- T_{ref} is any arbitrary NBS traceable delay inserted between the driver and receiver[2]

As stated earlier, the approach considered in this thesis is not aimed at replacing conventional timing calibration processes, but rather to enhance the overall timing accuracy and waveform quality, particularly at the interface between the DUT and the PEC. This technique can be harmonised with a conventional timing calibration, and will account for the effects of transmission path imperfections and the DUT and PEC loading.

Such an approach is useful, especially when close timing accuracy is needed, for example in AC parametric testing or in the prototype phase (characterization test) of high speed devices. Although this approach is aimed at low-end VLSI test systems (i. e. ASIC verification systems) it can equally well be employed in production testers to classify premium quality devices with a reduced guardband. Waveforms at the input pads of the DUT can be significantly improved so as to more closely determine the true performance of the DUT.

3.1.4 Automatic Calibration System

A tester's timing accuracy and resolution are leading parameters. To achieve sub-nanosecond accuracy in a high pin-count ASIC tester one cannot rely on transmission paths having equal physical lengths, and possibly equal electrical lengths. For instance, a one inch difference in path length causes about 100 ps timing difference. Consequently, testers must compensate for such variation by employing sophisticated automatic calibration techniques.

The goal of calibration is to ensure that all timed voltage transitions delivered to the pins of the DUT, and all times at which output data from the DUT are compared with expected data, are accurate in relation to a defined reference. The degree of this

[1] If timing generators are shared (Shared-Resources architecture).

[2] Coaxial cables are suggested for use as precision delays in Mydill's procedure.

accuracy determines the overall timing accuracy of the system. An IC undergoing test is connected to a tester's timing source through test system channels. Signals traveling through a channel must pass through a transmission line and driver or receiver connected to the pins of the DUT. The inevitable delays through circuits, and differences in transmission path length cause timing variation from channel to channel. Thus voltage transitions at the input pins or data detection at the output pins occur at different times even though they are supposed to be coincident, such timing offset is termed *skew*.

3.1.4.1 Calibration techniques

Essentially, a calibration system senses skewing between system channels and compensates for it by means of the variable delays in each system. Calibration can be performed by hardware, software or both. Two common hardware techniques used are [DEERR, 1983]:

- Manual adjustment
- Pre-measured cable

In manual adjustment, channel delays are measured with an oscilloscope. The delays are then manually adjusted to bring skew to within the system specification limits.

When pre-measured cable is used, an oscilloscope again measures delays, and a cable of appropriate length is placed in each channel path to equalise the delays. This method relies on the electrical rather than physical length of the cable.

Such manual methods are time-consuming. Consequently, the trend is toward automatic calibration. Instead of using an oscilloscope, internal detectors make the measurements, and software interprets the results and applies the necessary corrections. An automatic calibration method based on time domain reflectometry (TDR) seems to be almost ideal for VLSI test systems [SKALA, 1980; DEERR, 1983].

TDR is based on transmission line theory. A wave travelling through a transmission line terminated by anything other than the line characteristic impedance (Z_0), is partially reflected back along the line. If the line is terminated with an open circuit, the reflected wave's amplitude is equal that of the incident wave (reflection coefficient $\Gamma = 1$). What makes TDR so attractive is that in the test system the point of contact with the DUT pins is an open circuit when a device is not being tested. The TDR technique, therefore, can make measurements right up to the point at which the device pins are connected to the test system. However, when the DUT is inserted timing accuracy suffers because of uncertain DUT loading. This aspect has not been adequately taken into account in most calibration systems because the responsibility falls mid-way between the user and manufacturer of an IC tester. Generally, manufacturers or third parties offer design of customized DUT interface boards case-by-case, due to the difficulty of generalizing the requirements for each customer's application.

The calibration system, described in the next section, is designed to overcome this problem. Tester manufacturers need to provide improved facilities to give IC designers greater confidence in design verification and characterization test results.

3.2 THE PROPOSED CALIBRATION SYSTEM

Improvements of edge-placement accuracy and signal quality is realised by first modelling a transmission path between the PEC and the DUT using a SFG technique. The overall transfer characteristics of the transmission path or channel are then calculated over the frequency range of interest. Once the frequency response of each channel has been determined, we can:

1. optimize the waveform quality at any point along the transmission path and
2. determine the actual timing and (if desired) the waveform at the DUT output pads (or pins) from the measured values at the PEC receiver.

To demonstrate this approach, we investigate processes required to achieve the first goal. The second goal can be achieved by accounting for the influence of channel imperfections on the timing or pulse-shape.

To interface with the DUT output, we also propose that a unity gain buffer amplifier, fabricated in Thickfilm technology, be placed close to the DUT to drive and backmatch the transmission line. When the DUT input pins are being driven, the buffer will be bypassed by a PIN diode switch that can have as little as 1 Ω "on" resistance and less than 1 pF "off" capacitance. To minimize discontinuity, the buffer will be isolated from the transmission path by two more PIN diode-switches. This aspect requires further investigation as part of ongoing research.

The research reported in this thesis is not aimed at demonstrating a complete solution, but rather at assessing the feasibility of the approach and laying a thorough groundwork for further work.

3.2.1 An FDR Signal Source

A small-amplitude sinusoidal signal, with a *d.c.* level approximately half the required logic swing, is propagated to the DUT input pin. The reflection coefficient is measured at n harmonically related frequencies depending upon the operating test speed and the complexity of the DUT load model. At least n measurements are required for an n element load model, and the fundamental frequency is the test rate or clock speed used for that DUT. The signal source is the Pin Driver. Because only small amplitude sinusoids is used, we can operate the Pin Driver at higher frequencies than its logic specification. At the highest possible clock speed, the Pin Driver output waveform is almost sinusoidal, but the slew-rate limited frequency is inversely proportional to the Pin Driver output amplitude.

3.2.2 Complex Impedance Measurement

In most cases, the magnitude ratio of the reflected to the incident wave (the voltage reflection coefficient) is close to 1.0 because the loads, both DUT input impedance and PEC receiver input impedance, are typically high impedances. Magnitude information alone is inadequate to determine the load model, and phase measurement is essential. The phase detector is probably the most critical part of the system. HOER [1972], who has described a method of measuring complex impedance using only magnitude information, has shown that the phase relationship between the two sinusoidal voltages V_1 and V_2 can be completely determined from magnitude measurements of any three of the four vectors: $|V_1|$, $|V_2|$, $|V_1+V_2|$ and $|V_1-V_2|$. We propose to use a transmission line transformer hybrid circuit to obtain the sum and difference vectors. Magnitude measurements can then be performed using a peak detector circuit, which is considerably simpler than a conventional phase detector. The design of the measurement circuits is left to a later phase of this research. In this first phase, an early vector voltmeter (HP8405A Vector Voltmeter) has been used to demonstrate the main objective.

3.2.3 Transmission Path Model

A transmission path between a PEC and a DUT pin is modelled as cascaded blocks of linear N-port networks. Each N-port represents an element of that path, namely

- A Pin Driver as a signal source
- Discontinuity at a connection or junction
- Transmission line, uniform or non-uniform, either lossless or lossy
- A DUT input pin or a comparator of the PEC receiver, modelled as a load network
- A directional coupler, used to sample incident and reflected waves
- Other elements such as relays and switches

The cascaded N-port networks are represented using a signal flow graph technique.

3.2.4 Load Model Determination

Inserting a dummy DUT package in the test head will account for the particular package, permitting calibration right up to the die bonding pads. The dummy DUT is an empty package with every bonding pad shorted to the die mounting pad through a wire-bond or other appropriate process. This dummy package is used to define a reference plane for reflection coefficient measurement.

At this stage, we are using a linear time-invariant RLC network to model the DUT input impedance and package parasitics. Nonlinearities may be included later if necessary, but we believe that representing the DUT input impedance with such linear

approximation is adequate, especially for first-order correction. A load model can be obtained by adjusting the elements of a suitable canonical circuit to conform with the measured data; a direct search optimization algorithm being used to minimize an objective function formulated by a least squares method. This process is described in chapter 7.

3.2.5 The Waveform Quality

To ensure good quality signals at the DUT input pads, we propose, during initial calibration, to computer simulate the effects of the PEC–DUT propagation path on the stimulus waveform and thereby determine several supplementary waveforms that will be used to compensate for the channel discontinuities and imperfections, the energy coupled to the detector circuit, and the DUT loading. A suitable time domain waveform will be synthesized and added to the Pin Driver output, which, after propagating to the DUT, should have near-ideal waveshape and correspondingly improved edge-placement accuracy. This topic is discussed in chapter 8.

3.3 FREQUENCY DOMAIN OR TIME DOMAIN REFLECTOMETRY ?

To obtain a suitable compensation waveform for each channel environment, the characteristics of the channel must be determined. The channel model, from the output of the PEC to the end of the transmission path, can be determined during manufacture. Variation occurs when a custom DUT interface board is used, or the same interface board with a different package. However, the relevant information for a particular interface board or DUT package can be stored on-line without the need to recalculate the channel characteristics when a new device is tested. The only variable to be accounted for is the DUT itself.

The DUT loading effect can be measured using a reflectometer facility permanently built into each PEC. Such a facility must provide easy setup and require a minimum of additional hardware. There are several constraints on the reflectometer, such as space and cost. Space is a major limitation because the system must be incoporated into each PEC, and to be attractive its cost must be minimized.

Most of the techniques appropriate to this application are well known in microwave circles. Sophisticated elements such as the six-port reflectometer [ENGEN, 1977; 1978a; 1978b; TARR, 1983; HUNTER and SOMLO, 1985]employ power detectors and require complicated calibration. Despite their high accuracy and exellent high frequency performance, they are not suitable in their present form in space-limited and relatively low frequency applications.

These considerations constrain the system hardware to be simple and low cost. Such simplifications cannot be achieved without sacrificing accuracy. However, only approximation suitable for first-order correction is expected in this initial study. System

performance and accuracy can probably be further improved once the practicality of the proposed measurement system has been established.

3.3.1 Measurement Techniques

Since the incident wave contains no information about the load impedance at the end of the transmission line, the reflected wave must be employed. Circuits used to measure reflected waves may be classified as either bridges (balanced or unbalanced) or reflectometers [SOMLO and HUNTER, 1985]. Bridges are designed to compare two signals, one reflected from the unknown and one from a known termination, and provide an indication of the difference between them. When the circuit is adjusted for this difference to be zero, and therefore the indication to be null, the bridge is said to be balanced. Several bridge methods are described in a book by SOMLO and HUNTER [1985]. These methods are not suitable for our system because they require considerable time and external hardware to balance the bridge.

Reflectometers provide a direct measure of the signal reflected from the unknown. The significance of this signal must be determined by comparing it with that from a known termination substituted at the measurement port. Most reflectometer methods use a directional coupler to selectively couple the incident or reflected waves in a transmission line, making it one of the most useful components available for impedance measurement. Many reflectometer measuring circuits have been proposed and implemented [ENGEN and BEATY, 1959; HOLLWAY and SOMLO, 1969; 1973; LACY and OLDFILELD, 1973]. In this thesis, however, simple single and dual directional couplers have been investigated and implemented. Details of design and implementation are presented in chapter 5.

All the above methods fall into the category of frequency domain reflectometry. Another technique called Time Domain Reflectometry (TDR) has its origin in the techniques developed for the location of faults in cables carrying power or communication services [STEELE, 1985]. Frequency and time domain techniques are next described in detail.

3.3.1.1 Time domain reflectometry

TDR is a well-known method of obtaining information on discontinuities and loading effects in transmission lines. A schematic of a TDR system is shown in Figure 3.1.

The principle of TDR is to send a signal $f(t)$ along the line, and from the character and delay of the reflection deduce the character and location of the discontinuity.

The signal $f(t)$ and its frequency spectrum are related by Fourier transformations [SOMLO and HUNTER, 1985]

$$F(f) = \int_{-\infty}^{\infty} f(t)e^{-j2\pi ft}dt \tag{3.2}$$

$$f(t) = \int_{-\infty}^{\infty} F(f)e^{j2\pi ft}df \tag{3.3}$$

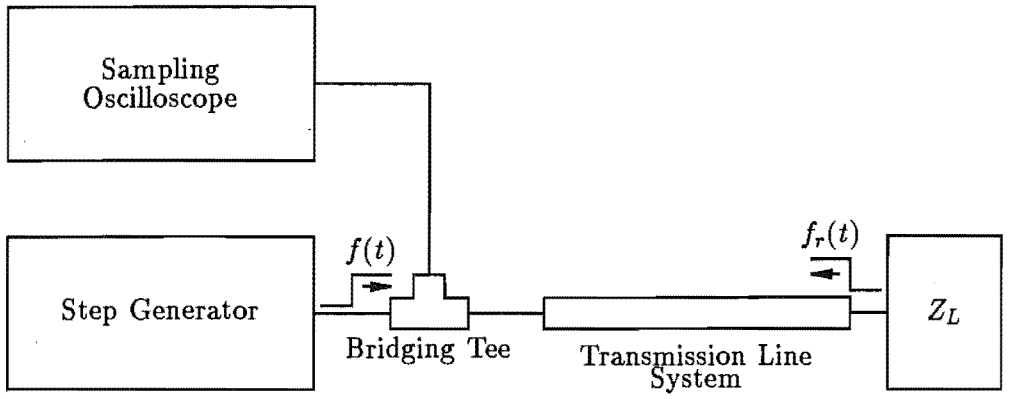


Figure 3.1 Time domain reflectometry system.

A discontinuity which results in a reflection coefficient $\Gamma_L(f)$ at the measuring port will produce a reflected signal $f_r(t)$ given by

$$f_r(t) = \int_{-\infty}^{\infty} \Gamma_L(f)F(f)e^{j2\pi ft}df \tag{3.4}$$

Suitably shaped pulses can be injected into a network and the locations of discontinuties determined from their return delays. Step functions, with spectra extending to zero frequency, have been most extensively used for such measurements [BRYANT, 1988]. It is convenient to send a step function, as shown in Figure 3.1, when the measurement is confined to the time domain. To enable reflections from adjacent discontinuities to be resolved, the rise time of the transmitted signal should be as small as possible (typically 50-150 ps).

Time domain measurements of this form suffer a number of disadvantages, many of which can be overcome by working in the frequency domain. A frequency dependent discontinuity, or a dispersive transmission line produces a distorted reflection, which can be difficult to interpret.

Modern time domain measurement is performed by injecting successive discrete spectral components and noting their modified amplitudes and phases on return from the discontinuity. Time information is obtained by taking a Discrete Fourier Transform (DFT) of the returned spectrum, thus yielding the same information on the discontinuity as is available from the step function method.

3.3.1.2 Frequency domain reflectometry

FDR requires a vector network analyzer to measure magnitude and phase of the incident and reflected waves. A discrete frequency domain test system is illustrated in Figure 3.2.

A number of frequencies can be applied and the time domain waveform obtained through Fourier transformation. The advantages of FDR include [HINES and STIREHELFER, 1974; BRYANT, 1988]:

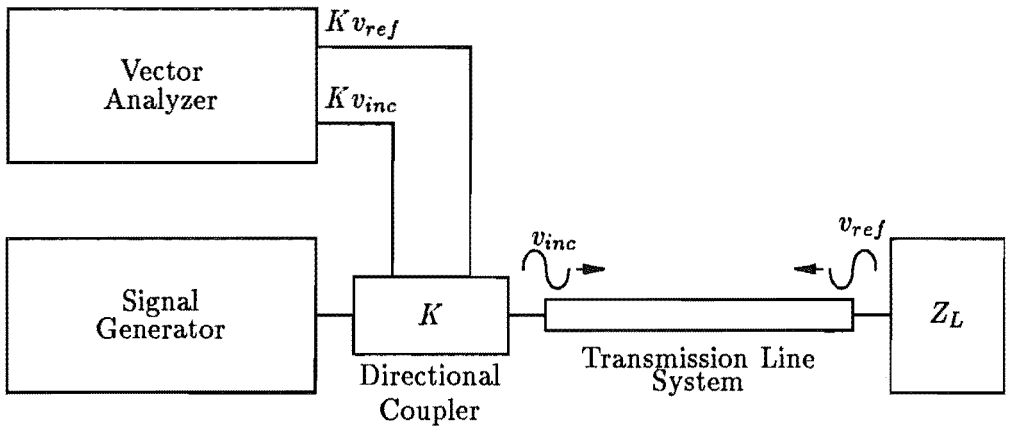


Figure 3.2 Frequency domain reflectometry system.

- An improvement in signal/noise ratio
- Waveforms other than a step can be simulated, such as an impulse
- Spectral shaping by windowing gives greater control of responses

Our application involves a relatively short propagation time, so if a TDR system is to be employed, it must have much wider bandwidth to resolve multiple reflections. Because location of discontinuities is not a primary concern in this investigation, and the effects on the waveform after travelling through the channel is a major interest, we have adopted an FDR technique.

Due to the bandwidth limitation of the Pin Driver (assuming no external source is used), only a limited number of discrete frequency measurements can be made. The results are used to optimize a lumped-element DUT load model, from which the frequency response of the load can be approximated analytically from the model.

3.4 SUMMARY

Figure 3.3 illustrates the proposed calibration system described in section 3.2. The major difference from conventional testers is the inclusion of a directional coupler, a waveform compensation unit, and a DUT output buffer.

The directional coupler is employed for the following purposes:

1. Timing alignment at the Pin Driver output;
2. To sample incident and reflected waves on the main line during FDR measurement.

The first purpose is outlined in section 5.1.4.6 and the second is investigated in detail in chapters 5 and 6.

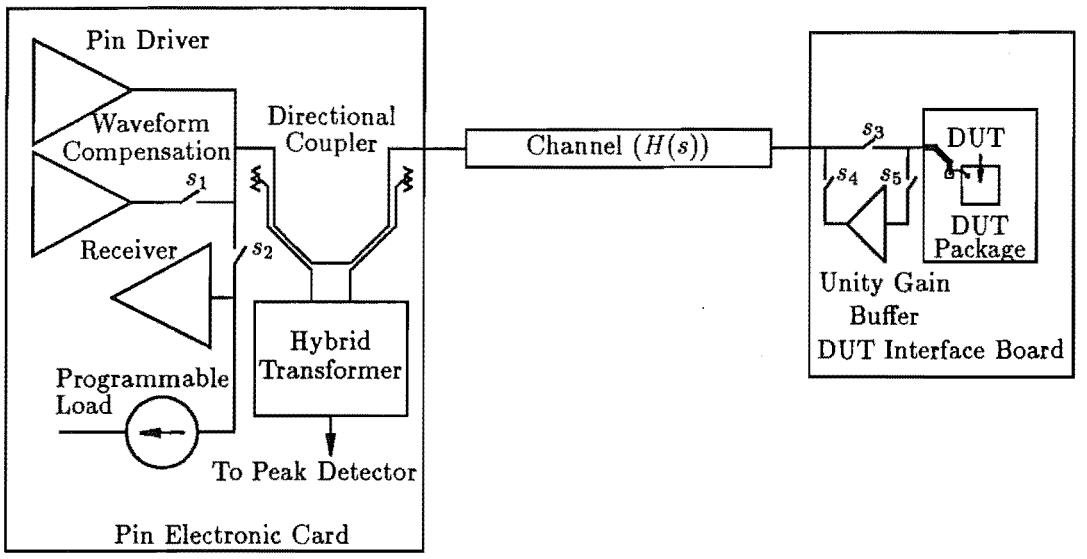


Figure 3.3 The proposed calibration system.

Due to the bandwidth limitation of the Pin Driver, only a limited number of discrete frequency measurements can be made. The results are used to optimize a lumped-element DUT load model, from which the frequency response of the load can be approximated analytically. This approach is described in chapter 7.

A unity gain buffer is used to drive and backmatch the transmission line in the receiving mode. It is isolated from the path, in driving mode, by two PIN diode switches s_4 and s_5. This aspect requires further investigation as part of ongoing research.

A compensation waveform can be computed from the channel and load characteristics. This technique should permit test engineers to optimize both timing and waveform quality at the DUT input pad, or any point along the transmission path. Chapter 8 presents a method of computing compensation for linear channels.

CHAPTER 4

FUNDAMENTAL THEORY

This chapter outlines some fundamental concepts of transmission line theory and related topics. Its purpose is to summarise the mathematical background, symbols, and notation used in this thesis. It is recommended reading for those not familiar with transmission lines, scattering parameters and SFG representation.

Various forms of transmission line geometry commonly used in high speed logic systems are presented in section 4.1. Basic concepts of complex impedance measurement are presented in section 4.2.

Sections 4.3 and 4.4 review the use of signal flow graph (SFG) analysis, network representation, and some useful techniques such as matrix renormalization and SFG reduction methods.

4.1 TRANSMISSION LINE GEOMETRY

Transmission line interconnections used in high speed logic systems, generally, consist of one, or a combination of the following transmission line types illustrated in Figure 4.1. All equations provided in this section are intended merely as a guide for rough estimation. Rigourous treatments of each case can be found in several texts, for example those by HOWE, Jr. [1974] for strip transmission lines, and EDWARDS [1981] for microstrip transmission lines.

4.1.1 Parallel Wire and Twisted Pair

Parallel wire, flat or ribbon cable for instance, is not normally used in such a high speed system. The characteristic impedance is given in equation 4.1 for $2r/d \ll 1$ [WALKER, 1990]. The characteristic impedance of a twisted pair is also approximated by equation 4.1. Figure 4.1 (a) shows the cross sections of a parallel wire and twisted pair, the latter being used sometimes in computer backplanes to reduce crosstalk between signal paths.

$$Z_0 = \frac{1}{\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\frac{2d}{r} \tag{4.1}$$

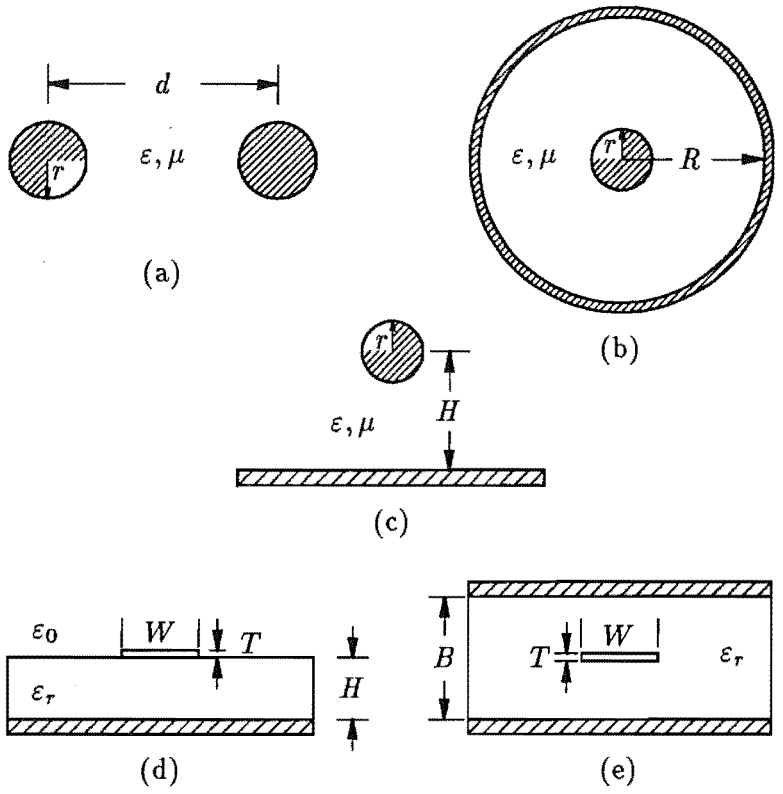


Figure 4.1 Cross sections of commonly used transmission lines (a) parallel wire and twisted pair (b) coaxial cable (c) wire over ground (d) microstrip (e) stripline.

where μ and ε are respectively the absolute permeability and permittivity of the surrounding medium.

4.1.2 Coaxial Cable

Widely used coaxial cables have characteristic impedances of 50, 75, 93, or 125 ohm. They are typically employed for long line lengths in the back plane of digital systems. The characteristic impedance is given by [BAKOGLU, 1990]

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\frac{R}{r} \tag{4.2}$$

4.1.3 Wire Over Ground

The wire over ground form is commonly used in packaging and interconnection of the DUT. The characteristic impedance is given by [BAKOGLU, 1990]

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon}}\ln\frac{2H}{r} \tag{4.3}$$

4.1.4 Microstrip Line

A microstrip line is a strip conductor separated from a ground plane by a solid dielectric. If the thickness, width of the line and the distance from the ground plane are controlled, the line will exhibit a predictable characteristic impedance. Because some energy is transmitted through the space above the dielectric, there are two natural modes of propagation in each direction. The resulting waves have two different velocities, which results in more complex reflections from discontinuities than is the case with lines having homogeneous dielectrics. This phenomenon is particularly important when Transverse Electromagnetic (TEM) directional couplers are fabricated in microstrip structures and results in a reduced isolation between conjugate ports.

The characteristic impedance of microstrip line can be obtained from various equations depending on the required accuracy, one of these equations is [BAKOGLU, 1990]

$$Z_0 = \frac{1}{2\pi}\sqrt{\frac{\mu}{\varepsilon_{eff}}}\ln\frac{4H}{d} \tag{4.4}$$

where

$$\varepsilon_{eff} = (0.475\varepsilon_r + 0.671)\varepsilon_0$$

and

$$d = 0.536W + 0.67T$$

for $W/H < 1.25$ and $0.1 < T/W < 0.8$. The accuracy is 5% for $2.5 < \varepsilon_r < 6$ [BAKOGLU, 1990]. The effective propagation delay τ in ns/m is given by

$$\begin{aligned}\tau &= \sqrt{\mu\varepsilon} \\ &= 3.33\sqrt{\varepsilon_{eff}}\end{aligned} \tag{4.5}$$

4.1.5 Strip Transmission Line

A strip line consists of a metal ribbon centered in a dielectric medium between two conducting planes. If the thickness and width of the line, the dielectric constant of the medium, and the distance between the ground plane are all controlled, the line will exhibit a characteristic impedance that can be held constant within ±5% [BLOOD, Jr., 1983].

The characteristic impedance of strip line also varies with the desired accuracy, only one equation is given [BAKOGLU, 1990]

$$Z_0 = \frac{1}{4}\sqrt{\frac{\mu}{\varepsilon}}\ln\frac{1+W/B}{W/B+T/B} \tag{4.6}$$

where $\varepsilon = \varepsilon_0\varepsilon_r$.

This equation proves accurate to 1–2% for $W/B > 1$ and to 5–6% for $W/B > 0.75$ provided that $T/B < 0.2$. The propagation delay τ in ns/m is given by

$$\tau = 3.33\sqrt{\varepsilon_r} \tag{4.7}$$

4.2 COMPLEX IMPEDANCE MEASUREMENT

This section summarises the basic theory of complex impedance measurement using a reflectometry method. All circuit elements in the measurement configuration are described using a scattering parameter (S-parameter) representation. A SFG method, which provides an easy way of illustrating complex networks, and some SFG reduction techniques used to simplify a complex network to a simpler one, are described in the next section.

4.2.1 Transmission Line Theory

For an elemental section of the line, as shown in Figure 4.2, the voltage and current relations may be written as

$$\begin{aligned} \frac{dV}{dz} &= -(RI + L\frac{dI}{dt}) \\ \frac{dI}{dz} &= -(GV + C\frac{dV}{dt}) \end{aligned} \tag{4.8}$$

where V and I are the voltage and current at distance z along the line. R, L, G, and C denote distributed series resistance, series inductance, shunt conductance, and shunt capacitance respectively. These quantities are given in their appropriate units per unit length. V and I in equation 4.8 are approximations, usable for frequencies where the separation of the conductors is very much less than the wavelength.

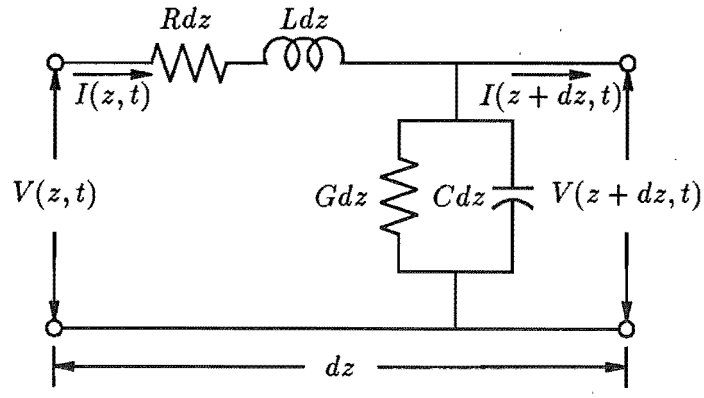


Figure 4.2 An elemental section of transmission line.

The general solution of equation 4.8 is

$$\begin{aligned} V &= ae^{-\gamma z} + be^{\gamma z} \\ I &= \frac{1}{Z_0}(ae^{-\gamma z} - be^{\gamma z}) \end{aligned} \tag{4.9}$$

where the propagation constant $\gamma = \sqrt{(R + j\omega L)(G + j\omega C)}$, and a and b are constants determined by assigning a specific value to V and I at some point along the line.

The propagation constant γ may be written as $\gamma = \alpha + \jmath\beta$, where α is the attenuation constant (nepers/m) and β is the phase constant (radians/m). In the case of a lossless line ($R = G = 0$) $\gamma = \jmath\beta = \jmath\omega\sqrt{LC}$. Since α is zero the wave propagates without attenuation. The wave with coefficient a, is called the incident wave, and is exponentially propagated in the positive z direction. The wave with coefficient b, called the reflected wave, is exponentially propagated in the negative z direction.

4.2.1.1 Lossless transmission line

The velocity of propagation through a lossless transmission line is independent of frequency and equal to the velocity of a plane wave in an infinite volume of the homogeneous, isotropic medium enclosing the conductors. The velocity of propagation v_p is therefore given by

$$v_p = \frac{1}{\sqrt{\mu_0\mu_r\varepsilon_0\varepsilon_r}} \tag{4.10}$$

where μ_r is the relative permeability (H/m), ε_r is the relative permittivity (F/m), μ_0 and ε_0 are the corresponding constant for free space $\mu_0 = 4\pi \times 10^{-7}$ H/m and $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m. Therefore

$$v_p = \frac{c}{\sqrt{\mu_r\varepsilon_r}} \tag{4.11}$$

where c is the velocity of light, approximately 3×10^8 m/s.

The voltage and current in the line are related by a characteristic impedance Z_0 which is resistive, independent of frequency, and equal to $\sqrt{L/C}$. For a homogeneous, isotropic medium the propagation delay per unit distance is $\tau = \sqrt{LC} = \sqrt{\mu_0\mu_r\varepsilon_0\varepsilon_r}$, the product LC being independent of the line geometry.

4.2.2 Impedance and Reflection Coefficient Concepts

By applying the definition of impedance to the line at point z, as shown in Figure 4.3, the impedance Z_{in} looking in the z direction is

$$Z_{in} = Z_0\frac{ae^{-\gamma z} + be^{\gamma z}}{ae^{-\gamma z} - be^{\gamma z}} \tag{4.12}$$

If $b = 0$ there is no reflected wave, and $Z_{in} = Z_0$, the line is said to be matched, and the impedance along the line is the characteristic impedance. If the impedance anywhere along the line is not equal to Z_0, the line is mismatched. In order to find a relationship between the coeffiecients a and b, the line is terminated with a load impedance Z_L at $z = 0$.

From equation 4.12, substituting $z = 0$ and $Z_{in} = Z_L$, gives

$$Z_L = Z_0\frac{a+b}{a-b} \tag{4.13}$$

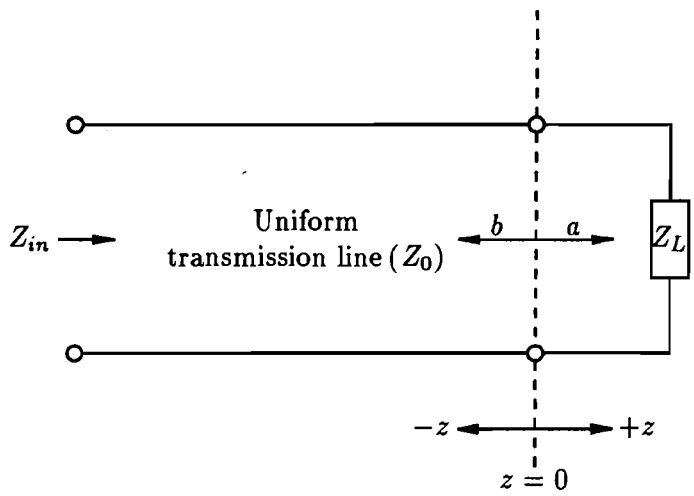


Figure 4.3 A uniform transmission line of characteristic impedance Z_0. terminated with load impedance Z_L at $z = 0$.

After rearranging, this becomes

$$\begin{aligned} \frac{b}{a} &= \frac{Z_L - Z_0}{Z_L + Z_0} \\ &= \Gamma_L \\ &= |\Gamma_L| e^{j\phi_\Gamma} \end{aligned} \tag{4.14}$$

where Γ_L is called the *reflection coefficient* of the load.

4.2.2.1 Input impedance along a transmission line

When there is no reflected wave on the line, the impedance at any point is Z_0. This is true for an infinite line, and also for a line which is sufficiently long that measurements can be made before any reflected wave returns.

If the terminated line in Figure 4.3 is cut at a distance $l = -z$ from the termination to create a pair of input terminals. The input impedance is found from equations 4.12 and 4.14 to be

$$Z_{in} = Z_0 \frac{Z_L/Z_0 + \tanh(\gamma l)}{1 + Z_L/Z_0 \tanh(\gamma l)} \tag{4.15}$$

When $Z_L = Z_0$, then $Z_{in} = Z_0$ for any length l, and therefore the line is indistinguishable at the input terminals from an infinite line. For a lossless line, equation 4.15 reduces to

$$Z_{in} = Z_0 \frac{Z_L/Z_0 + j\tan(\beta l)}{1 + jZ_L/Z_0 \tan(\beta l)} \tag{4.16}$$

Z_{in} is periodic with βl and is repeated at every multiple of $l = \pm\lambda/2$.

4.2.2.2 Input impedance described by reflection coefficient

The use of the reflection coefficient to describe the impedance transformation along the line is prefered due to its relatively simpler relationship.

Γ_{in} may be defined similarly to Γ_L in equation 4.12 by

$$\Gamma_{in} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{4.17}$$

and is the reflection coefficient, normalized to Z_0, at the input plane $l = -z$ of the transmission line.

From equations 4.12 and 4.17 we obtain

$$Z_{in} = Z_0 \frac{1 + \Gamma_{in}}{1 - \Gamma_{in}} \tag{4.18}$$

and

$$Z_L = Z_0 \frac{1 + \Gamma_L}{1 - \Gamma_L} \tag{4.19}$$

which when substituted into equation 4.15 gives

$$\begin{aligned} \Gamma_{in} &= \Gamma_L e^{-2\gamma l} \\ &= \Gamma_L e^{-2\alpha l} e^{-j2\beta l} \end{aligned} \tag{4.20}$$

This indicates that for a given terminating reflection coefficient Γ_L, the reflection coefficient Γ_{in} measured along the line will traverse an exponentially shrinking spiral on the complex Γ plane, and approach zero as distance increases from the load.

If the line is lossless ($\alpha = 0$)

$$\Gamma_{in} = \Gamma_L e^{-j2\beta l} \tag{4.21}$$

This is a function which is periodic with $l = \pm m\lambda/2; m = 1, 2, \ldots$, and on the complex Γ plane describes a circle with center at the origin and radius $|\Gamma_L|$. Equation 4.21 implies that remote measurement of Γ_L can be done provided that the length l is known. This is rather more difficult for a lossy transmission line because reflection coefficient transformation along the lossy line which has complex characteristic impedance is not a linear function of distance from the load. One solution for such problems, a parameter renormalization technique [WOODS, 1972; 1977a], requires some concepts for voltage and power wave reflection coefficients and this is described next. An understanding of voltage and power wave concepts is a very important step towards the proper use of scattering parameters.

4.2.3 Voltage- and Power-wave Concepts

Traditionally, the use of S-parameter network characterization has been mainly at microwave frequencies, and it has been customary to employ voltage-wave S-parameters

defined in terms of a real normalizing impedance (usually 50 Ω) [WOODS, 1972]. This is because S-parameters are normally measured in terms of the ratio of reflected to incident waves propagated in a transmission line having a characteristic impedance that, for most practical purposes, can be considered pure real. We call this a *real normalization* case.

However, in some applications the attenuation and reduction in the velocity of propagation, caused by finite conductor resistivity and other high frequency effects, must be taken into account and a lossless transmission line cannot be assumed. This leads to the concept of a voltage wave with complex normalization in which reflection coefficients greater than unity are encountered for passive networks.

A general definition of voltage reflection coefficient is given by

$$\Gamma_i^v \triangleq \frac{Z_i - \xi_i}{Z_i + \xi_i} \tag{4.22}$$

where $\xi_i = \varrho_i + \jmath\chi_i$ is a normalizing or reference impedance and Z_i is an input impedance of the i^{th} port, as shown in Figure 4.4.

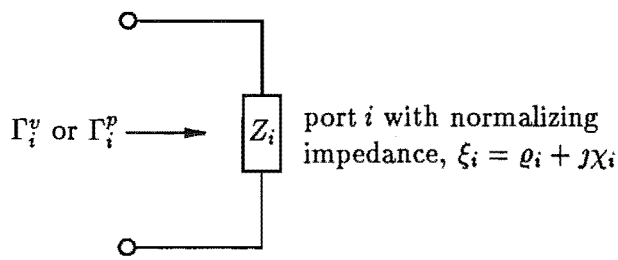


Figure 4.4 Voltage- and power-wave reflection coefficient defined at port i.

This definition leads to considerable complexity in power-transfer problems, because the two ideal conditions, an impedance match and maximum power transfer, are not coincident when the normalizing impedance ξ_i is complex. For the maximum power transfer case, a conjugate match is required, and this leads to some reflection; e. g. writing $Z_i = \xi_i^*$,

$$\begin{aligned} \Gamma_i^v &= \frac{\xi_i^* - \xi_i}{\xi_i^* + \xi_i} \\ &= -\frac{\jmath\chi_i}{\varrho_i} \end{aligned} \tag{4.23}$$

Power waves and generalized scattering matrix have been rigourously defined in a paper by KUROKAWA [1965]. These power waves were first introduced by PENFIELD, Jr. [1960]. YOULA [1961] studied the same waves for a positive real normalizing or reference impedance. The incident and reflected power waves a_i and b_i are defined by

$$a_i \triangleq \frac{V_i + \xi_i I_i}{2\sqrt{|\mathrm{Re}\xi_i|}} \tag{4.24}$$

$$b_i \triangleq \frac{V_i - \xi_i^* I_i}{2\sqrt{|\mathrm{Re}\xi_i|}} \tag{4.25}$$

where V_i and I_i are the voltage and the current flowing into the i^{th} port of a network and ξ_i is an arbitrary reference impedance of the i^{th} port, as illustrated in Figure 4.5.

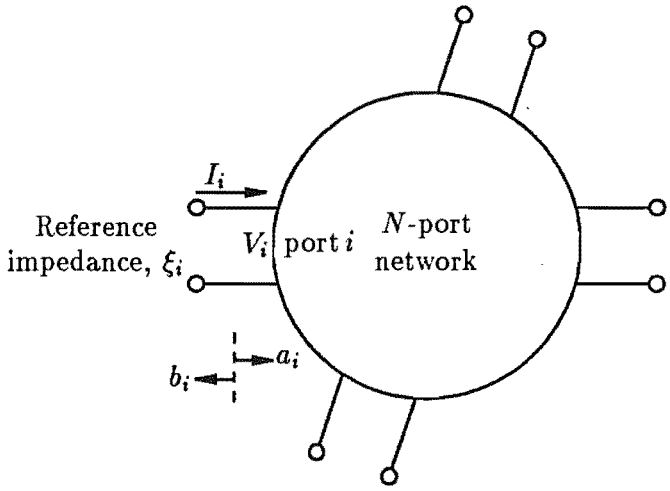


Figure 4.5 The incident and reflected power waves a_i and b_i defined at port i.

Equations 4.24 and 4.25 define a new set of variables, a_i and b_i, in terms of an old set, the terminal voltages and currents V_i and I_i. This definition is the result of just one of an infinite number of such linear transformations [KUROKAWA, 1965]. The expression for the relation between the a_i and b_i can be written as

$$b_i = S_{ij} a_j \tag{4.26}$$

where S_{ij} is an element of the generalized scattering matrix.

The power waves are defined in such a way that a conjugate match produces no reflection, and also in such a way that the incident wave carries the whole of the available power of the source and the reflected wave the total reflected power from the load. The power-wave reflection coefficient (Figure 4.4) is defined by [WOODS, 1972]

$$\Gamma_i^p \triangleq \frac{Z_i - \xi_i^*}{Z_i + \xi_i} \tag{4.27}$$

It has been shown that $|\Gamma_i^p|$ does not exceed unity for a passive load when ξ_i is complex [WOODS, 1972]. The reflection coefficient of an open circuit (oc) is $+1$ (the same as for voltage wave) but that for a short circuit (sc) is $-e^{-j\phi}$, where ϕ is the phase angle between ξ_i and ξ_i^*, as depicted in Figure 4.6. This means that short circuit and open circuit conditions are not π radians apart on the reflection coefficient circle. Consequently, the transformation of Γ_L^p through a line of complex ξ_i is not a linear function of distance.

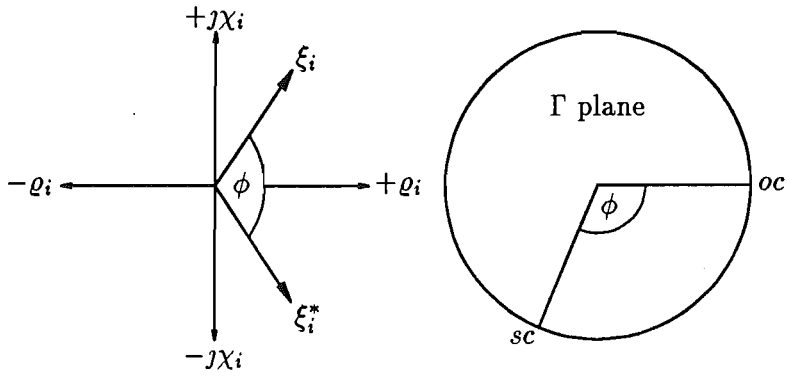


Figure 4.6 The reflection coefficient of short and open circuits for complex normalizing impedance.

If ξ_i is real and equal to the characteristic impedance of transmission lines connected to the ports of a network, then the definition of a_i and b_i reduces to that of the forward and reverse travelling waves on a lossless transmission line and S reduces to the microwave scattering matrix. Therefore the advantages of remote transmission line techniques can be used to measure the properties of the network and determine the generalized scattering matrix (i. e. the transformation of the reflection coefficient through the transmission line is a linear function of distance). The reflection coefficients defined by voltage-wave and power-wave (equation 4.22 and 4.27) are identical in this case.

For measurement purposes, the voltage-wave reflection coefficient has more direct application to the measurement process. Most S-parameter systems measure incident and reflected waves (separated by directional couplers) using a vector analyzer. The power waves are then obtained by mathematical transforms from the measured voltage-waves. Special care must be taken only when one wishes to normalize the parameters to complex port impedances. A method called matrix renormalization, described in section 4.3.4, allows one to measure all the parameters normalized to a real impedance, and then subsequently transform them using the required complex normalizing impedance.

4.3 SIGNAL FLOW GRAPH ANALYSIS

A *signal flow graph* is a symbolic, graphical method of writing a set of simultaneous linear equations, whereby the variables are represented by points or nodes and their interrelations by a directed graph giving a direct picture of signal flow. In a transmission line network which, generally, is a system of cascaded networks, the flow graph is simply constructed by joining together the flow graphs of the individual networks. The corresponding flow graph is particularly appropriate when the network is represented in scattering matrix form.

A well known application of the flow graph method is in the analysis of measuring techniques and the determination of residual errors, especially in microwave reflectometer systems. This method is applied in our analysis of the transmission path connecting the PEC and DUT. The analysis and correction for the reflection coefficient is achieved by the flow graph method.

4.3.1 Network Representation

To study one-port reflection coefficient measurement, methods are needed for representing and reducing to simpler configurations the networks employed in the measurement process. Although a linear load network may be fully described by its reflection coefficient normalized to a particular characteristic impedance, multi-port networks require more parameters for their description. A network may have any number of ports, but its parameters can be measured most easily by considering this network with only two ports, an input port and an output port, with all other ports terminated by known impedances, as shown in Figure 4.7.

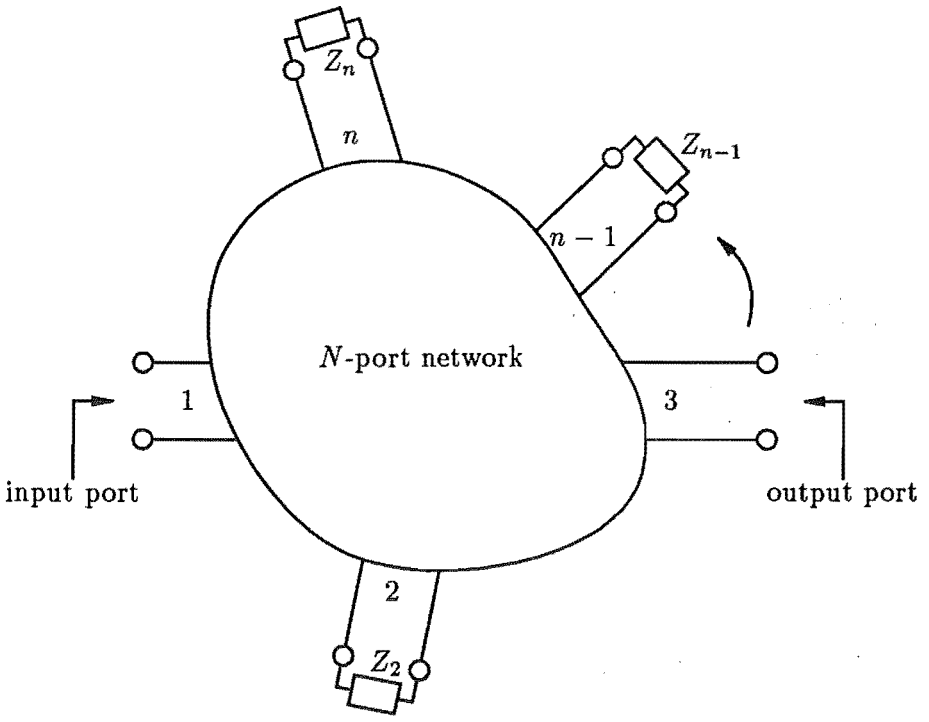


Figure 4.7 General N-port network.

Linear networks, or nonlinear networks operating with signals sufficiently small to cause the network to respond in a linear manner, can be completely characterized by parameters measured at the network terminals (ports) without regard to the contents of the network. To characterize the performance of such networks, any of several parameter sets can be used, each of which has certain advantages.

Parameter sets commonly used to characterize a two-port network are ABCD-parameter, Z-parameter, Y-parameter, H-parameter, G-parameter and S-parameter. S-parameters are commonly used in high frequency applications, particularly in the microwave region where direct measurements of port voltages and currents are often impracticable. Furthermore, short and open circuits required to obtain the Z, Y, H and G parameter sets are difficult to achieve over a wide frequency range. Discussions on the advantages and disadvantages of these parameter sets may be found in most network theory texts.

In our application, S-parameters are employed together with signal flow graph analysis. Before the author proceeds to present S-parameter representations of the transmission paths in the test head, their concepts and definitions are first outlined.

4.3.2 Signal Flow Graph and Scattering Parameter

The use of signal flow graphs for the solution of transmission line problems is most easily shown by considering the scattering matrix method of writing the network equations [KUHN, 1963]. In Figure 4.8 the general two-port network is shown as specified by its scattering matrix coefficients.

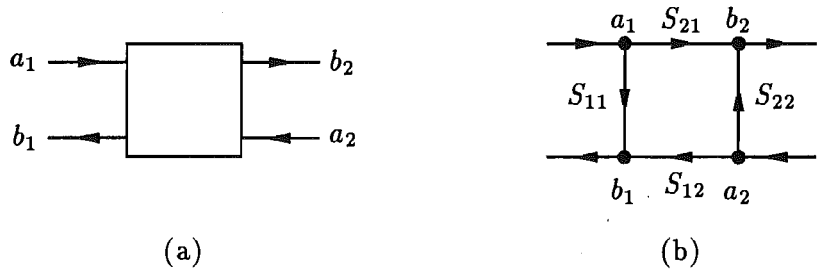


Figure 4.8 (a) A two-port network (b) its flow graph.

The coefficients a_1 and a_2 are the complex incident wave amplitudes at port 1 and port 2 respectively. The scattered wave amplitudes from the corresponding ports are represented by b_1 and b_2. The relationship of the scattered and the incident waves is written as a set of linear equations

$$\begin{aligned} b_1 &= S_{11}a_1 + S_{12}a_2 \\ b_2 &= S_{21}a_1 + S_{22}a_2. \end{aligned} \tag{4.28}$$

On this graph each port is represented by two nodes. Node a_n represents the incident wave at port n and node b_n represents the scattered wave from port n. A directed branch runs from each a node to each b node within the device. Each of these branches has a certain scattering coefficient from equation 4.28 associated with it. Each scattered wave, b_n is the linear sum of the scattered incident waves $S_{nj}a_j$,

shown in Figure 4.8 (b). Because b_n relies on superposition the technique described here is strictly valid only for linear time-invariant or time-varying systems in which superposition applies.

S_{11} is the reflection coefficient b_1/a_1 at port 1 when port 2 is terminated in a matched load ($a_2 = 0$). S_{22} is the reflection coefficient b_2/a_2 at port 2 when port 1 is terminated in a matched load ($a_1 = 0$). S_{21} is the transmission coefficient b_2/a_1 from port 1 to port 2 when port 2 is matched ($a_2 = 0$), and S_{12} is the transmission coefficient b_1/a_2 from port 2 to port 1 when port 1 is matched ($a_1 = 0$). In all reciprocal networks $S_{12} = S_{21}$.

4.3.3 Construction of Signal Flow Graphs

Figure 4.9 shows some simple flow graphs used as building blocks. These flow graphs are frequently encountered in transmission line networks.

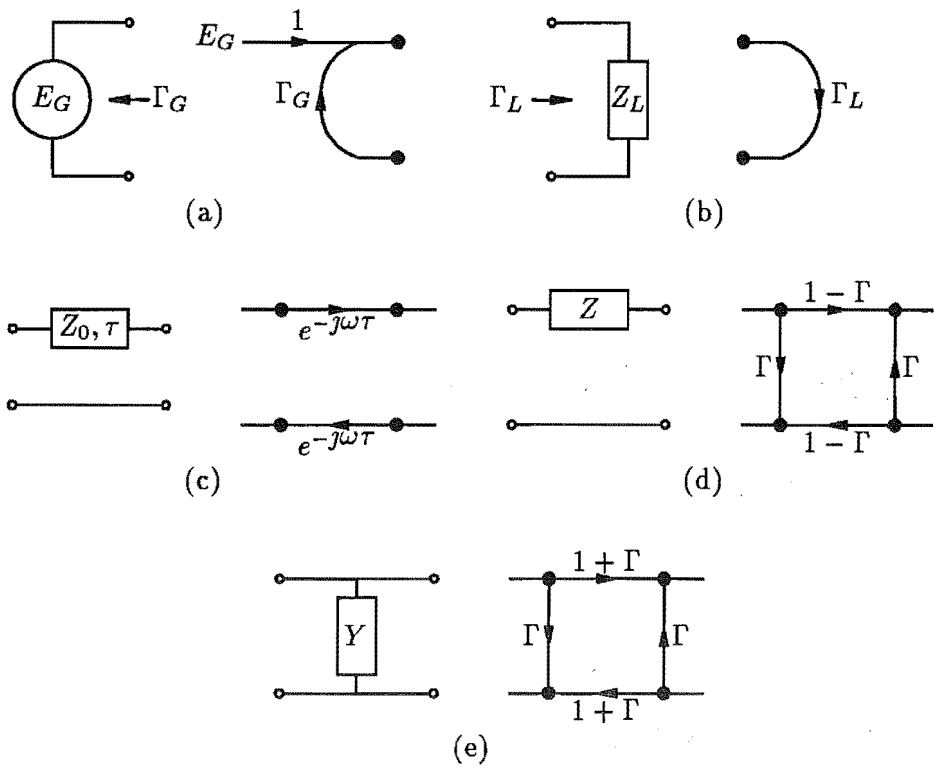


Figure 4.9 Some commonly used two-port networks and their flow graphs (a) a signal generator (b) a termination (c) a lossless, matched transmission line (d) a series impedance ($\Gamma = \frac{Z}{Z+2Z_0}$) (e) a shunt admittance ($\Gamma = \frac{-Y}{Y+2Y_0}$).

Networks are cascaded by joining their individual flow graphs with two connecting branches each of value 1 as in Figure 4.10. Three-port or four-port networks are cascaded in a similar manner to the two-port, as shown in Figure 4.10.

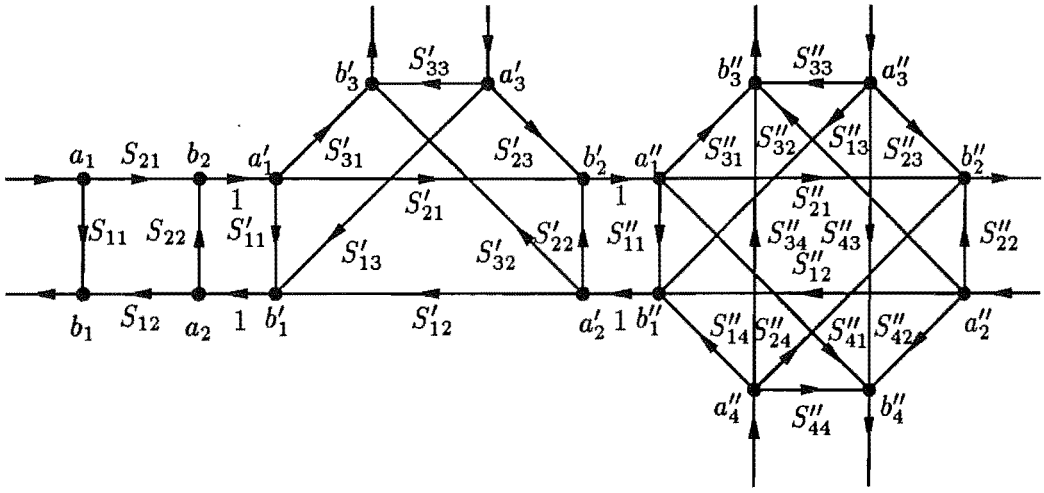


Figure 4.10 Cascaded flow graph of a two-port, a three-port and a four-port network.

4.3.4 Scattering Matrix Renormalization

A conventional method for measuring the $N \times N$ complex S-parameters is to use a 2-port automatic network analyzer (ANA). Several partial 2-port measurements must be performed with the ANA connected to various 2-port combinations of the network under test. In each of these 2-port measurements, the $N - 2$ unused ports of the network should, ideally, be terminated with perfectly matched loads. In practice, this requirement frequently cannot be met with sufficient accuracy, resulting in considerable error when reconstructing the S-matrix, especially those elements that are small in magnitude. These mismatch-induced errors may be eliminated by rigorously taking into account the finite reflections from $N-2$ mismatched auxiliary loads. Scattering matrix renormalization, described in this section, permits these partial 2-port measurements to be performed with arbitrary but known auxiliary loads terminated at the $N - 2$ ports. The S-matrix obtained from this method is then renormalized to the required set of normalizing impedances.

Although the matrix $\boldsymbol{S}$ containing the S-parameters of a network is associated with a set of characteristic impedances $\boldsymbol{\xi}$, it is possible to transform $\boldsymbol{S}$ into a matrix $\widetilde{\boldsymbol{S}}$ associated with a different set of characteristic impedances $\boldsymbol{\psi}$. This transformation is known as *matrix renormalization*, and is performed using [DROPKIN, 1983; TIPPETT and SPECIALE, 1982]

$$\widetilde{\boldsymbol{S}} = \boldsymbol{S} - (\boldsymbol{I} + \boldsymbol{S})\boldsymbol{\Gamma}(\boldsymbol{I} - \boldsymbol{S}\boldsymbol{\Gamma})^{-1}(\boldsymbol{I} - \boldsymbol{S}) \tag{4.29}$$

where $\boldsymbol{I}$ is the identity matrix, and $\boldsymbol{\Gamma}$ is a diagonal matrix of reflection coefficients of the loads $\boldsymbol{\psi}$ normalized to the impedances $\boldsymbol{\xi}$.

Other forms of this transformation are available, as are explicit expansions for 2, 3, 4, 5 and 6-port networks [WOODS, 1977a; 1977b; 1978]. The availability of the matrix

renormalization formula enables S, measured with arbitrary but known terminations connected to each port, to be transformed into $\tilde{S}$, the S-parameter set with the desired port impedances ψ. Terminations with the values ψ are therefore not required during the measurement.

When a network with known S and ξ has ports terminated in other impedances ψ, the application of matrix renormalization to find $\tilde{S}$ considerably simplifies the process of flow graph reduction discussed in the next section. For example, with terminations ψ the transmission from port n to port m is a complicated function of the elements of S, but is simply dependent on $\tilde{S}_{mn}$ of $\tilde{S}$.

4.4 SIGNAL FLOW GRAPH REDUCTION METHODS

Construction of the flow graph is only part of the problem. There remains the problem of finding the value of a wave at a certain node. Solutions for linear transmission line problems may be arrived at by a series of topological manipulations, or calculated using either algebraic or numeric methods which reduce a flow graph to a simpler form. These methods are refered to as *signal flow graph reduction* methods.

The purpose of flow graph reduction methods is to reduce a generally complicated flow graph to a single branch connecting two variables. The value of the branch is then the ratio of the variables. This will provide answers to questions such as "if a given signal enters port n, what signal will come out at port m?".

There are three commonly used methods for reducing flow graphs, as described below [SOMLO and HUNTER, 1985].

4.4.1 Topological Method

A topological method, based on four rules given by KUHN [1963]. These rules are applied successively to reduce a complicated flow graph to a simple one, ending in a single path connecting two nodes. The four rules are:

1. Branches in series multiply.
2. Branches in parallel add. For parallelism the arrows must point in the same direction. If they are pointing in opposite directions, a loop may be formed by duplicating a node according to rule 4.
3. A loop of value K attached to a node may be eliminated by dividing all incoming branches to that node by $1 - K$.
4. A node may be duplicated provided that every path on the original graph is maintained. Loops attached to a duplicated node will also be duplicated.

The above rules have been summarised by SOMLO and HUNTER [1985] and are repeated here without proof. An example using these rules can be found in Figure 8.11 of chapter 8.

4.4.2 Algebraic Method

This method is based on Mason's non-touching loop rule [MASON, 1953; 1956], which has been summarised by WARNER [1977]. The rule is given as:

$$T = \frac{P_1(1 - \Sigma_1 L_1 + \Sigma_1 L_2 - \ldots) + P_2(1 - \Sigma_2 L_1 + \Sigma_2 L_2 - \ldots) + \cdots}{1 - \Sigma L_1 + \Sigma L_2 - \ldots} \quad (4.30)$$

where T is the coefficient of a single path linking two variables (i. e. $b = Ta$), and where

- P_1 is one path from a to b.
- P_2 is a different path from a to b, etc.
- ΣL_1 is the sum of all first-order loops.
- ΣL_2 is the sum of all second-order loops, etc.
- $\Sigma_1 L_1$ is the sum of all first-order loops not touching P_1.
- $\Sigma_1 L_2$ is the sum of all second-order loops not touching P_1.
- $\Sigma_2 L_1$ is the sum of all first-order loops not touching P_2.
- $\Sigma_2 L_2$ is the sum of all second-order loops not touching P_2.
- etc.

A path is the product of all branches encountered *en route* following the directions of arrows and not passing any node more than once. There may be many distinct paths from node a to node b. A first-order loop is a closed path in the directions of the arrows, not passing over any node more than once. Its value is the product of all branches traversed. A second-order loop is the product of any two first-order loops which do not touch at any point. A third-order loop is the product of three non-touching first-order loops, and so on.

To illustrate this technique, we consider the SFG of a two-port network terminated with an arbitrary load Γ_L, as shown in Figure 4.11.

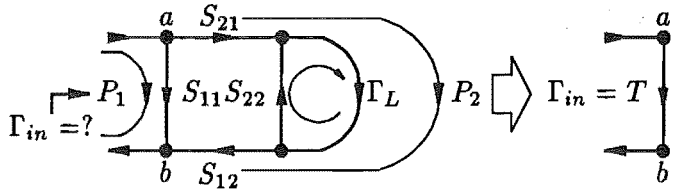


Figure 4.11 An example of SFG reduction using non-touching loop rule.

There are two paths from a to b, $P_1 = S_{11}$ and $P_2 = S_{21}\Gamma_L S_{12}$. There is only one first-order loop ($S_{22}\Gamma_L$), therefore the sum of all first-order loops $\Sigma L_1 = S_{22}\Gamma_L$.

The sum of all first-order loops not touching P_1, $\Sigma_1 L_1$, is also equal to $S_{22}\Gamma_L$. But because the loop $S_{22}\Gamma_L$ touches P_2, the sum of all first-order loops not touching P_2, $\Sigma_2 L_1 = 0$.

The required coefficient $T = \Gamma_{in}$ is then obtained by substituting the values of $P_1, P_2, \Sigma L_1, \Sigma_1 L_1$, and zero for all other terms (since there is no second- or higher-order loop) into equation 4.30, to give the result

$$T = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{4.31}$$

4.4.3 Matrix Method

This method is suitable for implementation on digital computers and it is chosen to be used in our analyses. The method first suggested by ABRAHAMS [1966] has been simplified by MUNRO and McMORRAN [1970]. The algorithm is simple, effective, and easy to implement.

The N nodes in the flow graph are numbered from 1 to N. An $N \times N$ matrix (transmittance matrix) is formed with the branch values S_{ij} in the i, j position. If the desired answer is the ratio of the signal at the q^{th} node to that at the p^{th} node, the matrix is then augmented by an extra $(N+1)^{th}$ row and column containing zeros except in the positions $(q, N+1)$ and $(N+1, p)$, which contain values of 1. This additional $(N+1)^{th}$ row and column can be thought of as a source node, and is connected to node p, while a sink node is connected to node q. The source and sink nodes are connected to the desired node pair by branches of values 1, as shown in Figure 4.12.

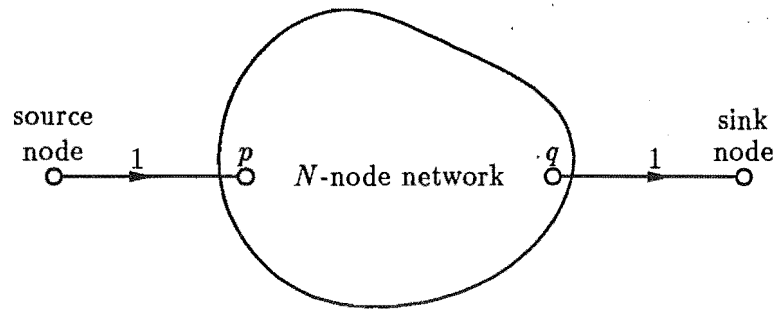


Figure 4.12 The source and sink nodes are connected to nodes p and q of the N-node network respectively.

The augmented matrix is reduced in the following manner:

- For $j = 1, \ldots, N$ scan column j for row $i = j+1, \ldots, N+1$.
- For all nonzero entries in column j add $S_{ij}S_{jk}/(1 - S_{jj})$ to S_{ik} for $k = j+1, \ldots, N+1$.
- The required answer is given by element $S_{N+1,N+1}$.

where indices i and k pertain to residual nodes and j to a node which disappears in the reduction. The residual transmittance between nodes i and k is the sum of all residual transmittances in the original graph, with those transmittances going through node j modified by (1− the loop transmittance).

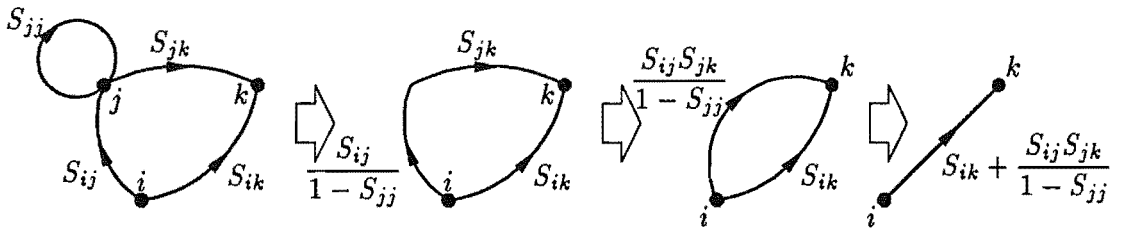


Figure 4.13 An example to illustrate SFG reduction using matrix method.

The reduction is accomplished by eliminating every node, one node at a time, in the original SFG. If a node, for example node j in Figure 4.13, has a self-loop attatched to it, then every incoming transmittance to this node must be divided by $(1 - S_{jj})$. This is similar to rule 3 (loop elimination) in the topological method. The product $S_{ij}S_{jk}$ represent a path that passes through node j from node i to node k. This is similar to rule 1 in the topological method.

If there is a path from node i to node k ($S_{ik} \neq 0$) in the original graph, then the new path between these two nodes is the sum of the result from the process described above (i. e. $S_{ij}S_{jk}/(1 - S_{jj})$) and the original path since they are parallel. This is rule 2 in the topological method.

The original $N \times N$ matrix can be reused to determine the transmission between other node pairs after relocating the sink and source nodes to the new node pair.

Implementation of the above reduction rules is straightforward on a digital computer. Both numerical and symbolic procedures have been implemented and tested. The algorithm is derived from BASIC code given by SOMLO and HUNTER [1985, appendix A, pp. 201~202]. The symbolic procedure is implemented using MAPLE[1]. The aim of this symbolic procedure is to provide a cross check on the results during the development of the program. The advantage of using symbolic computation to find the results is that we can obtain an explicit formula and then substitute element values to get numerical results (provided that the original graph has not been changed). In numerical computation, flow graph reduction must be carried out each time we compute the ratio of any node pair. The symbolic procedure is presented in appendix F. The numerical procedure is written in C programming language, and the codes are not given since it is based on the same algorithm as in the symbolic procedure.

[1]A system of symbolic mathematical computation developed by University of Waterloo, Canada.

CHAPTER 5

DIRECTIONAL COUPLER DESIGN AND IMPLEMENTATION

The FDR measurement, described in chapter 3, requires a directional coupler to separate incident and reflected waves. Two prototype directional couplers have been designed and implemented to investigate feasibility of the proposed calibration system. Both prototypes were constructed, using Thickfilm-Hybrid (TFH) technology, in the Microelectronic Laboratory, University of Canterbury, New Zealand.

These prototypes were primarily designed to examine the characteristics of a practical directional coupler. The final design construction, size, and fabrication technology may be different from these prototype couplers. Dimensions may be given in both SI and British units.

Section 5.1 introduces a theory of electromagnetic coupling between parallel-coupled transmission lines, their parameters and responses both in steady state and transient. Sections 5.2 and 5.3 describe design and implementation of the prototype directional couplers. Test results for their electrical characteristics are presented in section 5.5.

5.1 THEORY OF DIRECTIONAL COUPLER

When a signal is propagated along parallel conductor lines, electromagnetic coupling between the lines leads to a serious crosstalk problem. This effect was investigated many years ago [CARSON and HOYT, 1927], and the early investigations were directed toward eliminating rather than using this effect [OLIVER, 1954]. Such electromagnetic coupling, when analyzed mathematically, has led to practical devices, called *directional couplers*, having a simpler and cheaper structure than had previously been possible.

Directional couplers find wide application in microwave networks and systems [MALHERBE, 1988]. They perform a variety of functions, such as splitting and combining power in mixers, sampling power from sources for level control, dividing power among a number of loads, or separating incident and reflected signals in network analyzers. In this thesis, the application of a directional coupler to separate incident and reflected signals will be considered.

5.1.1 Directional Electromagnetic Couplers

Directional coupling between parallel transmission lines has been studied with well-known results [OLIVER, 1954; MONTEATH, 1955; JONES and BOLLJAHN, 1956]. Appendix A presents the analysis of parallel-coupled lines, which shows that for a matched parallel-coupled line system, the coupled wave will travel in a direction opposite to that of the incident wave. The analysis employs the following assumptions [OLIVER, 1954]:

- The line loss is negligible.
- The conductor sizes and spacings are infinitesimal compared with the wave length.
- All currents are confined to the conductor surfaces.
- The propagation medium is homogeneous, isotropic, and has negligible loss.
- The lines are balanced with respect to their surroundings and the coupling between them is symmetrical.

For the application described in this thesis, with appropriate transmission line geometry, all these assumptions will be satisfied. Directional couplers in the form of paralled-coupled transmission lines will be investigated in detail in the following subsections.

5.1.2 Parallel Coupled-Line Directional Coupler Parameters

Figure 5.1 indicates port notations and parallel-coupled-line directional coupler system functions.

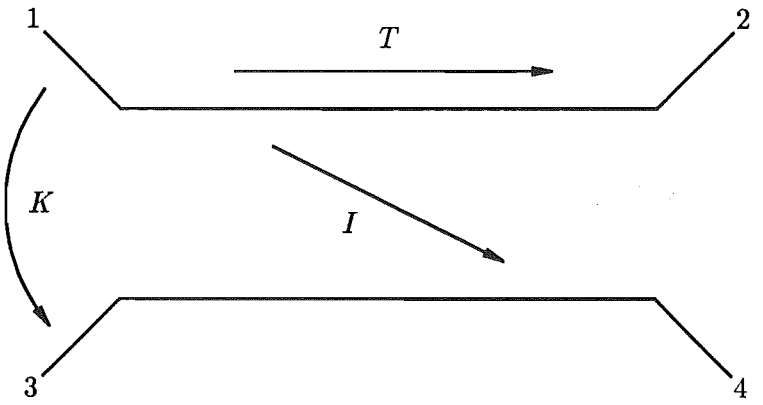


Figure 5.1 Port notations and system functions of a parallel-coupled-line directional coupler.

The major parameters are defined as [EDWARDS, 1981]

- Coupling factor ($K = V_3/V_1$)
- Transmission factor ($T = V_2/V_1$)
- Isolation factor ($I = V_4/V_1$)
- Directivity factor ($D = I/K = V_4/V_3$) when excitation is applied *only* at port 1

It is common to quote these quantities in decibels, for example, a 20–dB coupler. This is a loose description, since the voltage of port 3 is −20 dB relative to that of port 1. Note that D is derived from the ratio of two system functions but is *not* itself a system function. For ideal couplers $I = 0$ therefore $D = I/K = 0$ and the power is split between ports 2 and 3. This applies quite accurately to coaxial and stripline couplers for which TEM modes exist, but it is rather inaccurate for microstrip couplers of simple parallel-coupled construction. The following discussion will assume TEM propagation modes exist since strip transmission line will be employed.

5.1.3 Steady-State Response

The steady-state sinusoidal response of a directional coupler has been investigated by many people [OLIVER, 1954; JONES and BOLLJAHN, 1956] and the analysis is presented in appendix B. The results for voltage at port 2 and 3 are repeated here:

$$V_2 = \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta} \tag{5.1}$$

$$V_3 = \frac{jK\sin\theta}{\sqrt{1-K^2}\cos\theta + j\sin\theta} \tag{5.2}$$

where $\theta = \beta l = \omega l/v_p = 2\pi f l/v_p$
β = phase constant (radians/m)
v_p = velocity of propagation (m/s)
l = coupled length of the lines (m)
θ = electrical length of the coupled section(radians)
K = coupling factor.

Figures 5.2 (a) and (b) show the magnitude and phase of voltages at port 2 as a function of θ for various values of K whereas the magnitude and phase of voltages at port 3 are illustrated in Figures 5.3 (a) and (b) respectively. The responses are repeated at nf_m, where $n = 2, 4, 6, \ldots$ and f_m is the mid-band frequency.

5.1.4 Transient Response

The transient response of a parallel-coupled-line directional coupler is important, particularly for digital engineers, because it relates to crosstalk effects in high speed digital systems. These effects have been extensively examined [JARVIS, 1963; FELLER

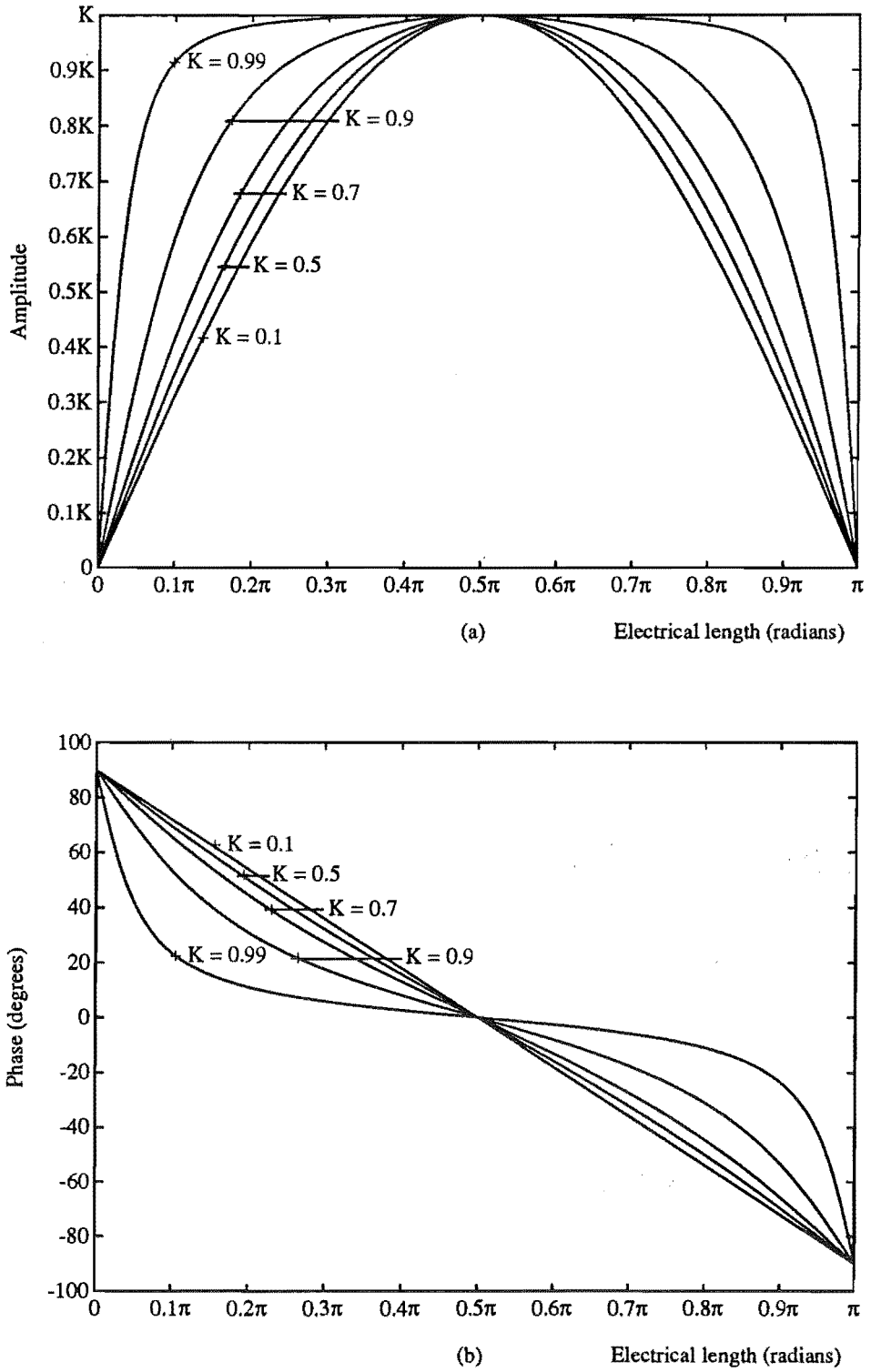


Figure 5.2 Steady-state responses at port 2 (S_{21}) plotted versus the electrical length (θ) (a) magnitude (b) phase.

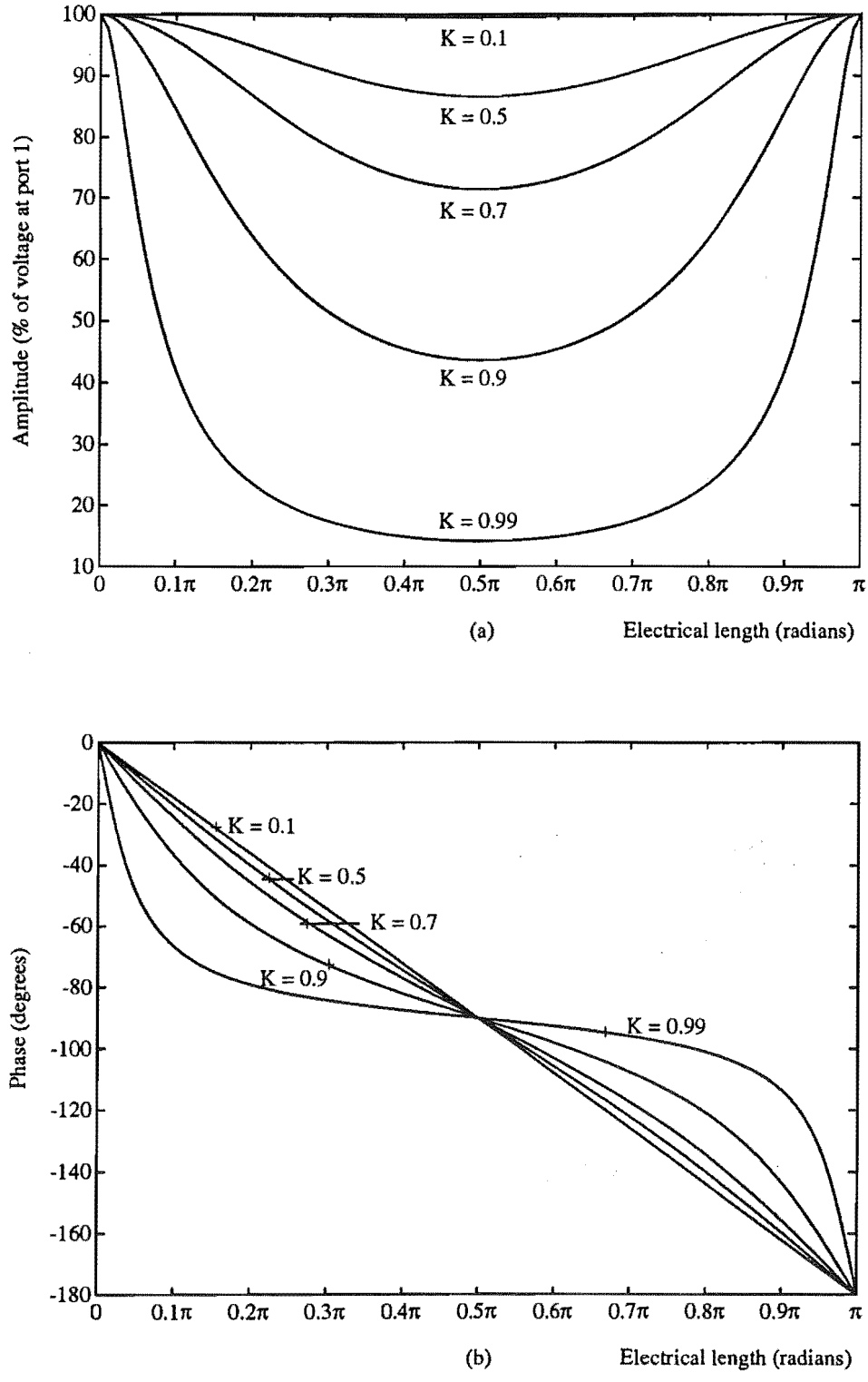


Figure 5.3 Steady-state responses at port 3 (S_{31}) plotted versus the electrical length (θ) (a) magnitude (b) phase.

et al., 1965; CATT, 1967; DeFALCO, 1970]. This section discusses the coupler transient responses for a weak coupler ($K \ll 1$) and how they can be used to align timing at the output of the Pin Driver.

5.1.4.1 A rigorous method

For a weak coupler, equation 5.2 becomes

$$\frac{V_3}{V_1} = \frac{\jmath K \sin\theta}{\cos\theta + \jmath \sin\theta} \tag{5.3}$$

The delay time in coupled lines l metres long is $\tau_0 = l/v_p$, and substituting $\sin\theta = \frac{1}{2\jmath}(e^{\jmath\theta} - e^{-\jmath\theta})$ and $\cos\theta = \frac{1}{2}(e^{\jmath\theta} + e^{-\jmath\theta})$, equation 5.3 becomes

$$\frac{V_3}{V_1} = \frac{K}{2}(1 - e^{-\jmath 2\sin\theta}) \tag{5.4}$$

Substituting $\theta = \omega\tau_0$ gives

$$\frac{V_3}{V_1} = \frac{K}{2}(1 - e^{-\jmath 2\omega\tau_0}) \tag{5.5}$$

and for $s = \jmath\omega$

$$\frac{V_3}{V_1} = \frac{K}{2}(1 - e^{-2s\tau_0}) \tag{5.6}$$

The coupler output voltage can be obtained by finding the Laplace transform of the input signal and multiplying with the impulse response from equation 5.6. The time domain waveform is the inverse Laplace transform of the product of the input signal and the impulse response.

5.1.4.2 A simple method

There is a simpler and quicker way to obtain the coupler output waveform for a weak coupler. Because the impulse response of the weak coupling directional coupler is simple, the time domain waveform of the output can be obtained by shifting the input waveform, in time, by $2\tau_0$, and inverting the phase of this waveform. The sum of the unshifted input waveform and the shifted, inverse phase waveform will yield the output waveform. The resultant output waveform has also been attenuated by a constant $K/2$. This can be explained by considering the impulse response of the directional coupler as a transfer function block as shown in Figure 5.4.

This transfer function block can be separated into two parallel blocks as shown in Figure 5.5. So, the input signal is separated into two paths; one passes through an attenuation of $K/2$ and the other passes through a delay in time of $2\tau_0$, and the phase shift by 180°, and is also multiplied by an attenuation $K/2$. The output waveform is the sum of these two paths.

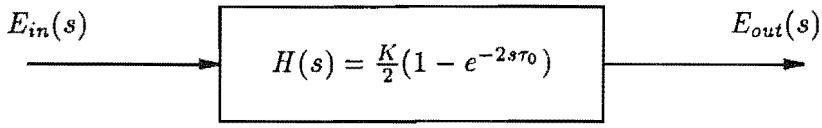


Figure 5.4 Transfer function block of a directional coupler.

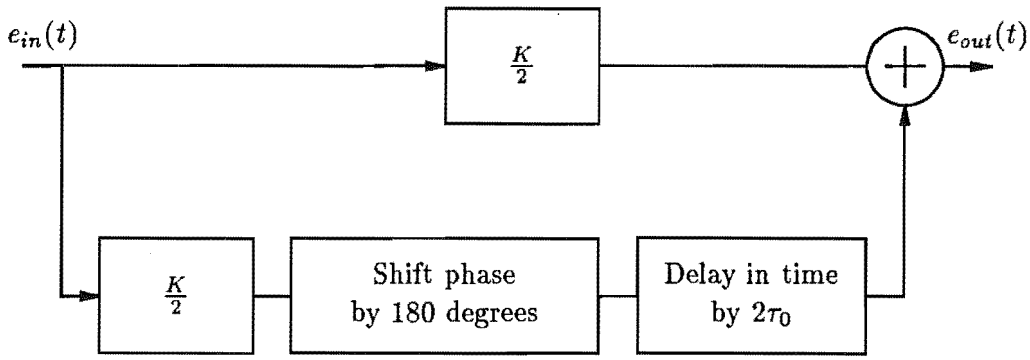


Figure 5.5 Equivalent transfer function blocks.

5.1.4.3 Ideal step pulse response

An ideal step input of amplitude A is fed into the matched system directional coupler, as shown in figure 5.6.

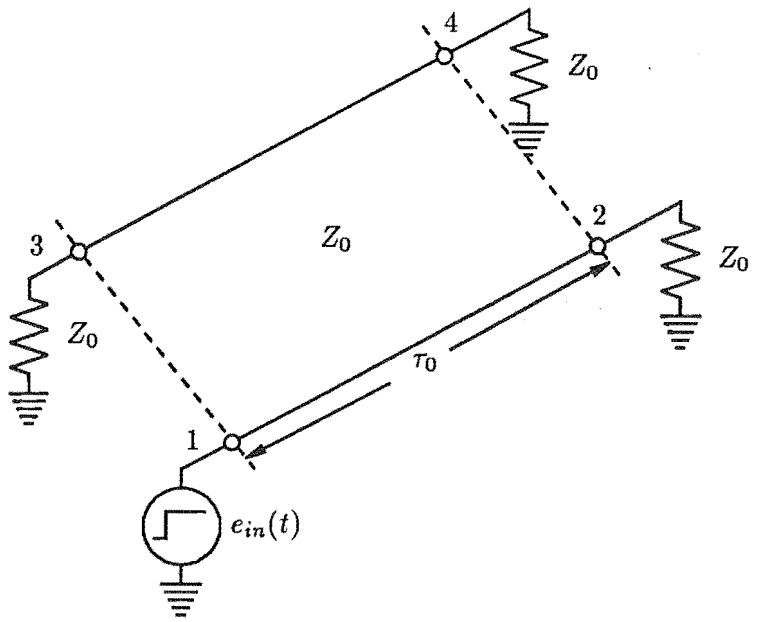


Figure 5.6 Matched system parallel-coupled lines driven with an ideal step at port 1.

The incremental induced wave generated at any point along the coupled line begins as soon as the rate of increase of the voltage of the wavefront becomes significant at that point. The induced wave begins to appear at port 3 as the leading edge of the wavefront enters port 1, at $t = 0$. The amplitude of the induced wave at time 0^+ is $KA/2$. The edge of wavefront travels from port 1 to port 2 in time τ_0, and during this time the incremental induced wave is coupled at every incremental line length and travels back to port 3 on the coupled line. Hence the amplitude of the induced wave is constant until the wavefront of the inducing wave has reached port 2, and it remains constant until the final portion of the backward induced wave has traveled from port 4 to port 3, taking a time of τ_0. The waveforms at port 1 and 3 are shown in Figure 5.7.

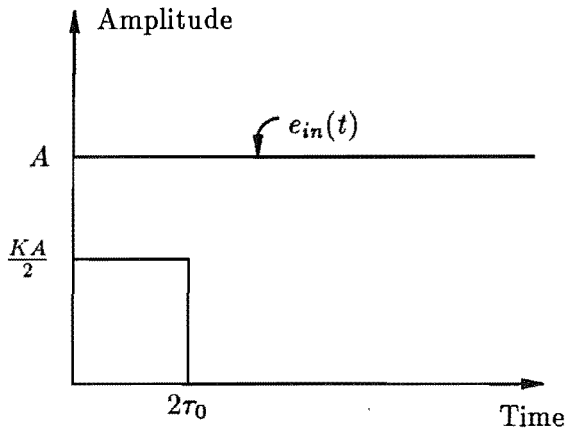


Figure 5.7 Directional coupler step response, the input amplitude of the step is A V.

This output waveform is similar to the reverse (or backward) crosstalk observed in a high speed digital system. If the material used in the transmission path of a test head is homogeneous and isotropic, induced waves created by mutual inductance and mutual capacitance are equal, and forward coupling is eliminated. Only backward coupling is present, giving an output at port 3, and none at port 4.

5.1.4.4 Ideal ramp pulse response

The typical waveform used in a digital system is not an ideal step. These pulses have finite transition times. When the input pulse transition time is changed, the output waveform also changes. Figure 5.8 shows coupled voltages at port 3 for different input pulse transition times.

The dependence of the peak amplitude at port 3 on the input transition time is shown in Figure 5.9. The output amplitude varies with the transition time of the input pulse when the transition time is longer than $2\tau_0$. When the input pulse transition time is less than $2\tau_0$ the output pulse amplitude depends only on the input amplitude and coupling factor.

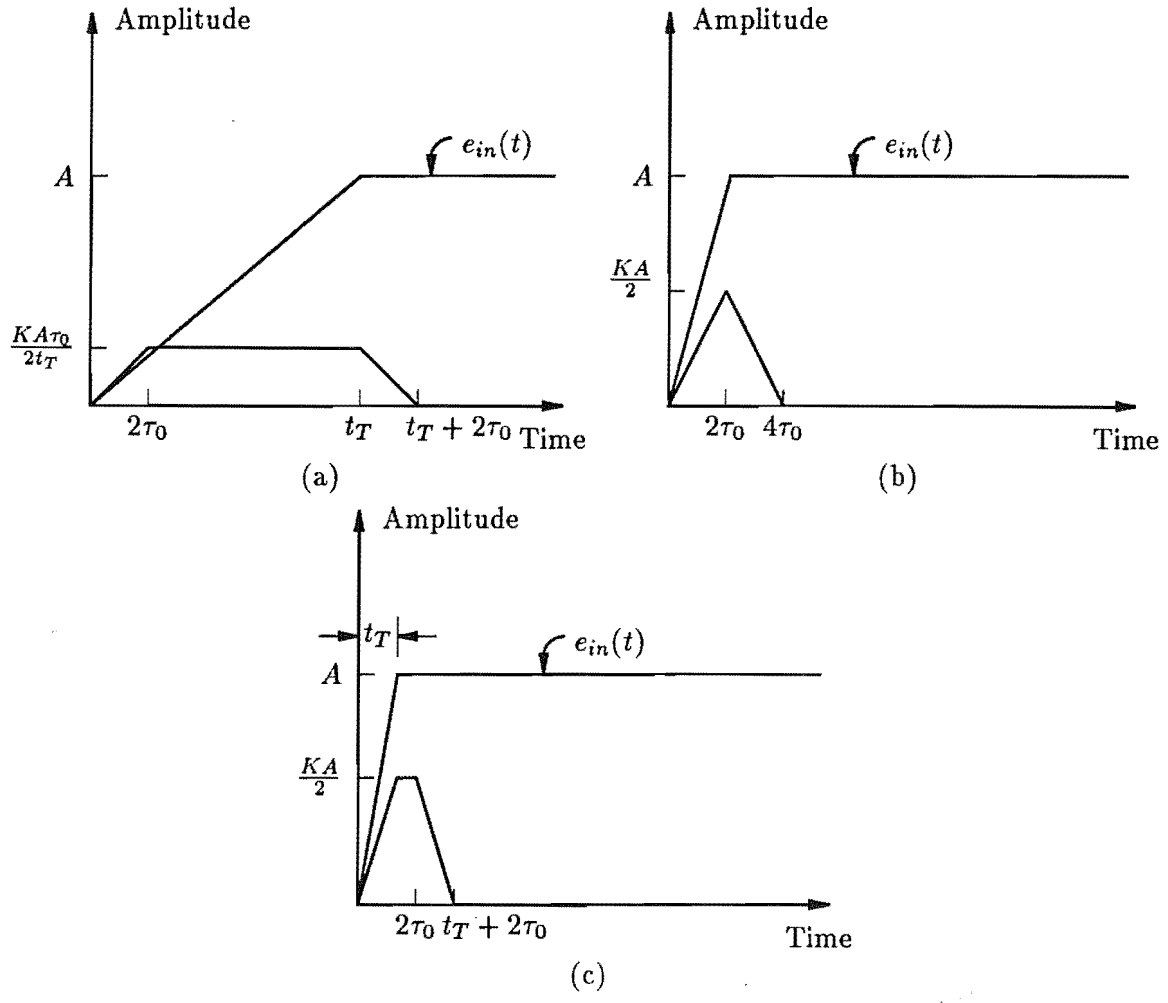


Figure 5.8 Ideal ramp pulse responses for different input transition times (a) $t_T > 2\tau_0$ (b) $t_T = 2\tau_0$ (c) $t_T < 2\tau_0$.

5.1.4.5 Arbitrary pulse response

In practice there is no ideal step or ramp pulse, principally because of stray capacitances at the output of the pulse generator and the input of the system that limit the system bandwidth. The response of the directional coupler to these practical pulses can be obtained by the same methods as described above, or by computer simulation of the analytical results.

Figure 5.10 shows typical waveforms at port 3 when an exponentially rising pulse waveform is fed into port 1. The response waveform in Figures 5.10 was obtained using the simple time domain method described in section 5.1.4.2. The amplitude relationship with rise time is similar to that of the ideal ramp response.

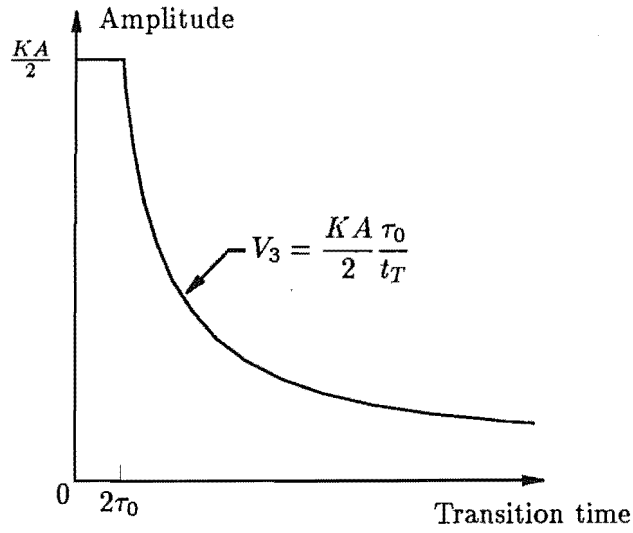


Figure 5.9 Relationship of the output amplitude and the input transition time.

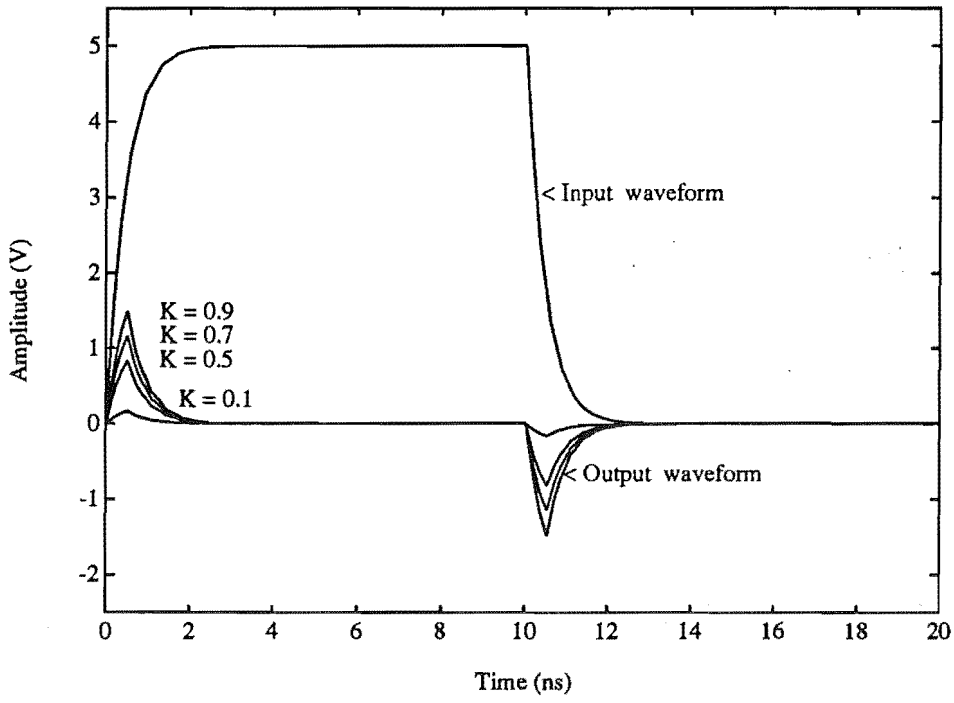


Figure 5.10 Exponential pulse responses, the input amplitude is 5 V with rise time (10%–90%) = 1 ns and the coupler propagation delay $\tau_0 = 0.5$ ns, coupling factor $K = 0.1$, 0.5, 0.7, and 0.9.

5.1.4.6 Timing alignment using directional coupler

The transient response of the directional coupler can be used to align pulse timing at the output of the Pin Driver. Figure 5.11 illustrates how this can be implemented.

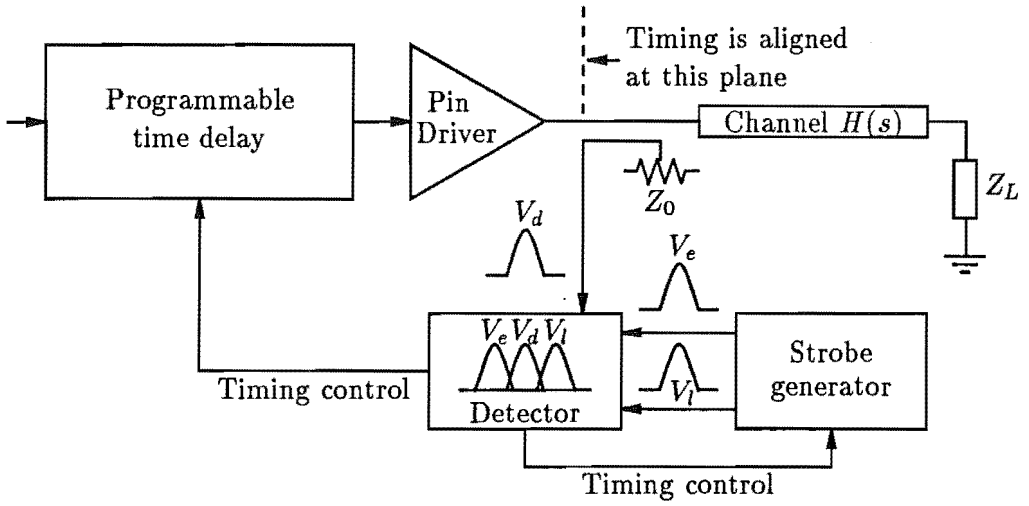


Figure 5.11 Timing alignment using directional coupler transient responses.

The fastest transition time of the Pin Driver should be used in this process. The detector circuit produces two strobe signals, namely the early (V_e) and late (V_l) strobes. These strobes are used to locate the position of the edge of each Pin Driver output. The two strobes have a fixed time separation equal to the half-amplitude width of pulse V_d. By exclusively ORing V_d with V_e and V_l, a difference (or offset) is obtained in proportion to the asymmetrical time offset of V_d relative to V_e and V_l. The offset will be zero when a negative feedback (timing control) loop drives the strobes to equally straddle V_d.

One channel is selected as a reference channel, the strobes are shifted in time until the coupled pulse (incident wave only) from the directional coupler is centered between these two signals. The strobes are then fixed, and used as a reference to calibrate the remaining channels by adjusting timing delay in each channel until the edge timing aligns with the reference channel. This method will guarantee that all transitions are coincident at the output of the Pin Drivers, but the design of the detector circuit requires further investigation.

5.2 DESIGN OF THE PROTOTYPE DIRECTIONAL COUPLER

In practice, the specifications for a directional coupler include information on the following [EDWARDS, 1981]:

- Transmission line geometry
- Characteristic impedance
- Coupling factor at the mid-band frequency
- The lowest acceptable directivity and isolation factors

From data in this form the designer will decide upon the structural dimensions of the coupler.

5.2.1 Coupler Geometry

Parallel-coupled-line directional couplers consist of two or more parallel transmission lines coupled between a common pair of ground planes or the equivalent. Figure 5.12 shows the cross section of a variety of geometries that can be used to realize coupled-lines sections.

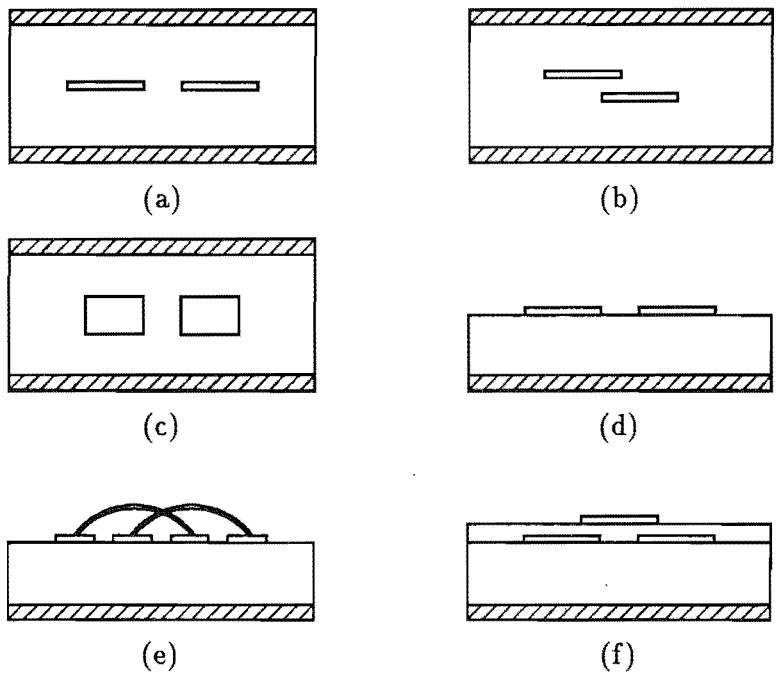


Figure 5.12 Various cross sections of commonly used coupled-lines directional coupler.

Figure 5.12 (a), (b), and (c) are stripline configurations, (a) is commonly used for weak couplers, (b) is for tighter couplers and (c) is for high power couplers.

Figure 5.12 (d), (e), and (f) are microstrip configurations, (d) is for weak couplers, while (e) (the so-called Lange coupler) and (f) will provide tighter couplers up to -3 dB.

In this thesis, only a simple single-section quarter-wave directional coupler, in the form of a strip transmission line or tri-plate configuration, will be discussed. Although a multi-section coupler gives a wider bandwidth, it is not considered for implementation in this initial study.

The first prototype is a simple single section directional coupler and the second is a dual directional coupler. The second coupler has been designed and built because the first had unsatisfactory performance (especially above 500 MHz) in the FDR experiment described in chapter 6.

Circuit diagrams and port notation for both types of coupler and their associated signal flow graphs are shown in Figure 5.13 and 5.14 respectively. The dual directional coupler flow graph of Figure 5.14 (b) is a simplified form of the six-port flow graph, assuming that the internal terminations of port 5 and 6 are perfect and there is no interaction between ports 3 and 4. In these flow graphs, and some complex flow graphs in the following discussion, scattering coefficients are omitted for clarity and simplicity.

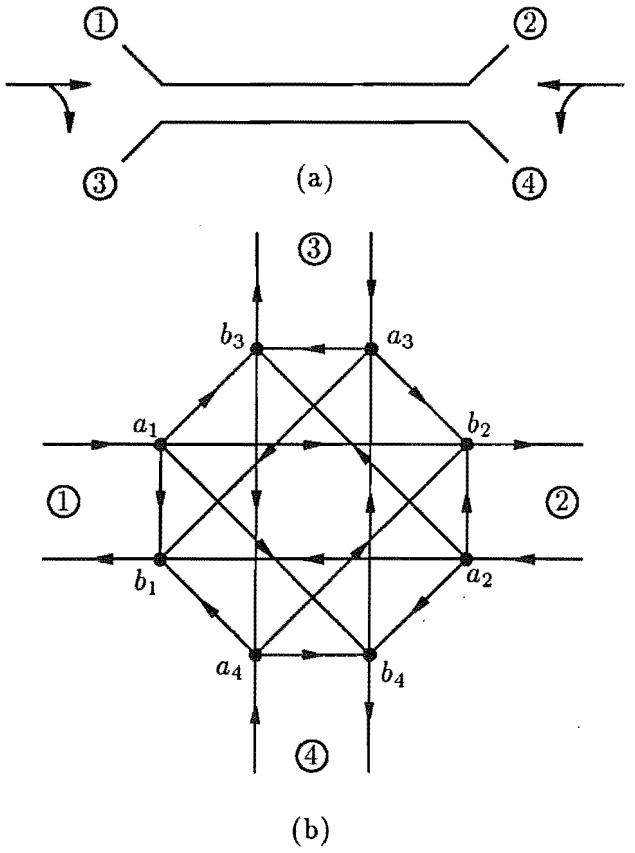


Figure 5.13 A coupled-line directional coupler (a) circuit diagram (b) its signal flow graph.

In the preferred implementation of the dual coupler, a triple-line structure as shown in Figure 5.14 (b) was not employed. Instead, a cascade of two parallel-coupled lines was employed. This structure gives higher isolation between ports 3 and 4 since the isolation factor depends on the matching condition of internal terminations which can be easily controlled. Figures 5.15 (a) and (b) depict the circuit diagram and flow graph of the second prototype coupler. Assuming perfect internal terminations and an infinite isolation between ports 3 and 4, the complete flow graph can be reduced to a cascade of two 3-port networks, shown in Figures 5.15 (b).

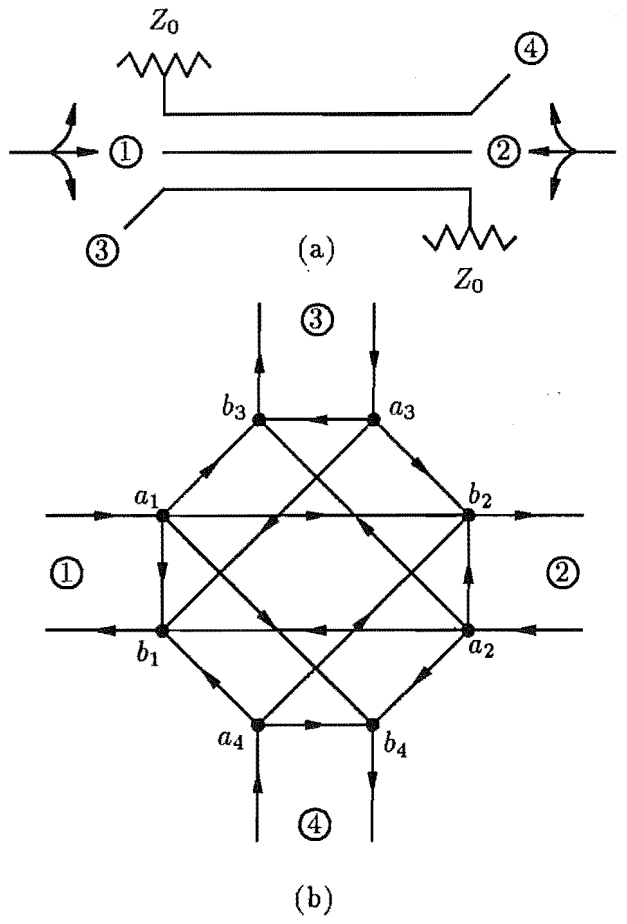


Figure 5.14 A dual directional coupler (a) circuit diagram for a triple-line structure (b) its signal flow graph.

5.2.2 Coupling Factor Selection

Because the coupler is permanently in the channel, a weak coupling factor is desired, so as to maintain signal integrity in the main line. For example, if $K = 0.1$ (a -20-db coupler) only 1% of the incident energy will be coupled across at the mid-band frequency. This will permit virtually non-invasive parameter and edge timing control on a continuous basis if desired. Because an ideal coupler has frequency-independent Z_0, no unwanted reflections can result from such monitoring, regardless of the chosen K. The minimum practical value of K will depend upon the sensitivity of the detector circuit and the noise level in the channel (which is expected to be -80 to -120 dBV).

It is desired that the coupler frequency response cover the frequency range of interest, in this case from *d.c.* to 1 GHz. The mid-band frequency of the first prototype was chosen to be 500 MHz, and 1 GHz for the second. The intended operating frequency range in the FDR experiment is from 100 MHz to 1 GHz. Because the second prototype coupler has a larger bandwidth than the first one, the magnitude response at the

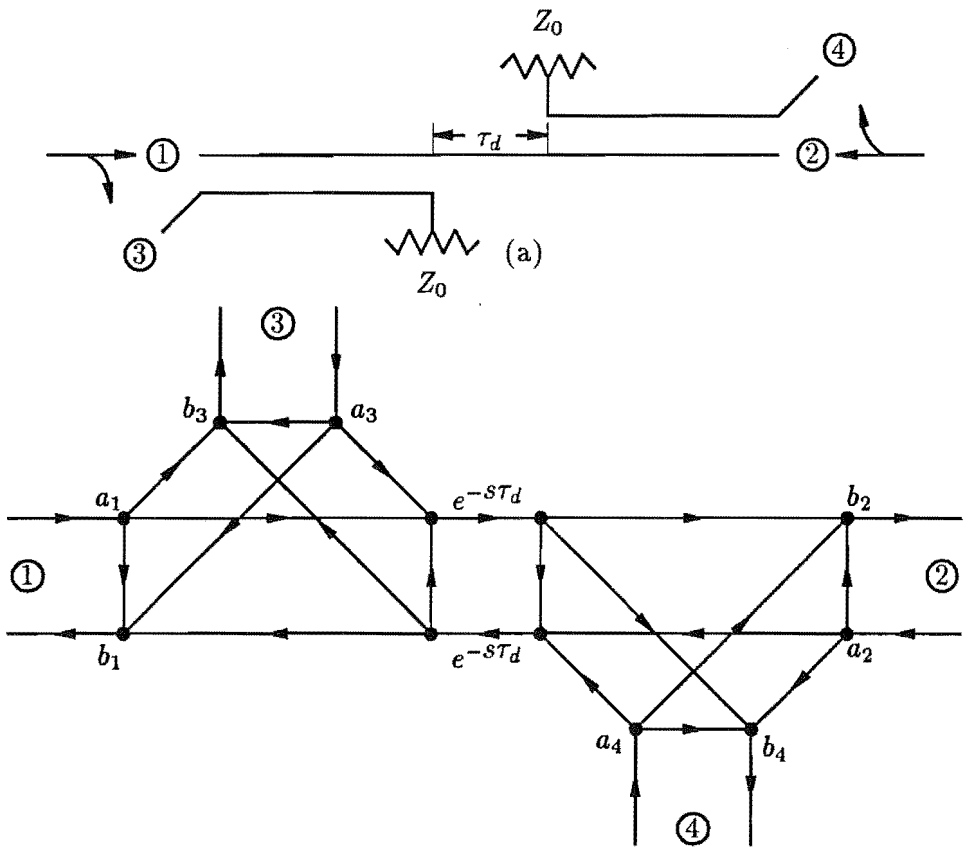


Figure 5.15 Actual implementation of the dual directional coupler (a) circuit diagram for a cascade of two parallel-coupled lines (b) its signal flow graph.

lower-end frequency is relatively smaller. The author therefore decided to increase the coupling factor of the second coupler to $K = 0.2$, and so overcome the increasing uncertainty (due to finite directivity at high frequency) from which the first coupler suffers. Figure 5.16 shows a comparison of magnitude responses of both prototype couplers over the frequency range of interest.

The physical length of the coupler depends upon the dielectric constant of the medium surrounding the transmission line, and this will determine the time delay or phase delay of that coupler at the selected mid-band frequency.

5.2.3 Design Methodologies

There are a number of software packages available to help design and simulate microwave circuits. At University of Canterbury, none of these was available at the time when the author started designing the prototype couplers. Since the design is not complex, the author carried out all the design manually.

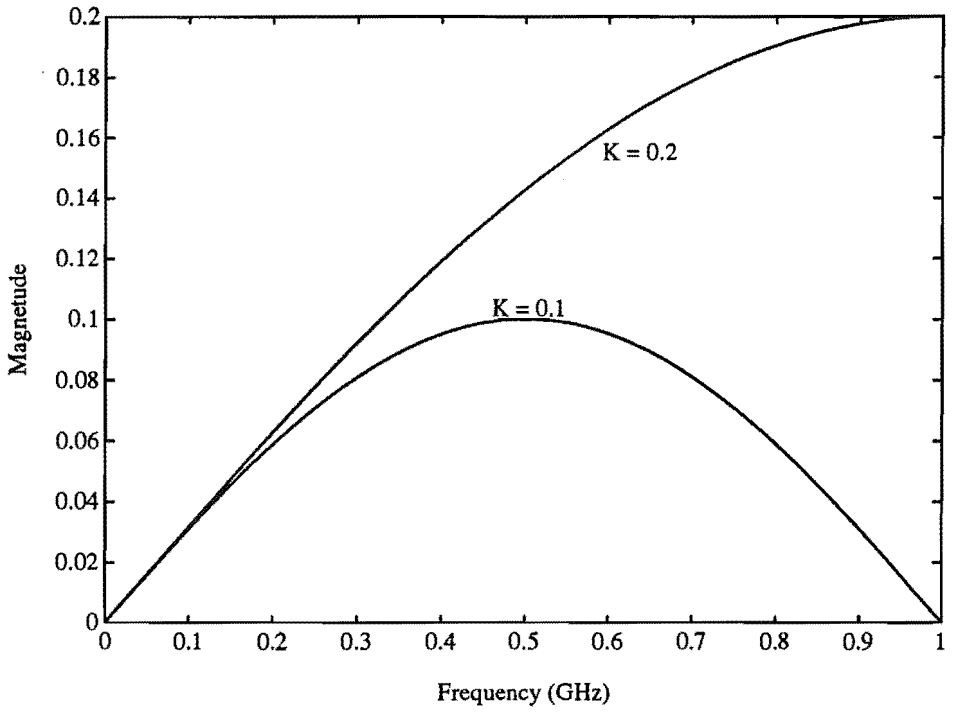


Figure 5.16 A comparison of ideal magnitude responses ($|S_{21}|$) of the two prototype directional couplers, from *d.c.* to 1 GHz.

There are three unknown parameters when designing a directional coupler, the coupled-line width (W), spacing (S), and the physical length (l) of the coupled section. Other known parameters are:

- Coupling factor;
  - For the single directional coupler, $K = 0.1$ (a 20-dB coupler) at 500 MHz (mid-band frequency).
  - For the dual directional coupler, $K = 0.2$ (a 13.9-dB coupler) at 1 GHz (mid-band frequency).
- Characteristic impedance; $Z_0 = 50\,\Omega$
- Conductor thickness; $T = 8$–$12\,\mu$m ($9\,\mu$m will be used)
- Groundplane spacing; $B = 1.279$ mm
- Relative dielectric constant of Al_2O_3; $\varepsilon_r = 9.3$

	Width (*mil*)	Spacing (*mil*)	Physical length (*mil*)
Single coupler	10.2(11)	25.4(25)	1959.8(1960)
Dual coupler	11.5(12)	13.8(14)	979.9(980)

Table 5.1 Parameters for the prototype directional couplers.

5.2.3.1 The even- and odd-mode characteristic impedances

The even- and odd-mode characteristic impedances relate to the coupling factor, K as follows:

$$\begin{aligned} Z_{oe} &= Z_0\sqrt{\frac{1+K}{1-K}} \\ Z_{oo} &= Z_0\sqrt{\frac{1-K}{1+K}} \end{aligned} \tag{5.7}$$

From equation 5.7, we find that

- $Z_{oe} = 55.277\,\Omega$ and $Z_{oo} = 45.227\,\Omega$ for the single directional coupler and
- $Z_{oe} = 61.237\,\Omega$ and $Z_{oo} = 40.825\,\Omega$ for the dual directional coupler.

5.2.3.2 Coupler line width and spacing

The ratios of W/B and S/B can be determined with the aid of Figures 5.17 and 5.18 [COHN, 1955b], approximating the T/B ratio (0.007) to be zero.

The values of W and S were calculated from the ratios W/B and S/B obtained from the nomograms, and are listed in Table 5.1, where all the parameters are presented in $mil = 0.001$ inch.

Note from Table 5.1, that the ratio of $W/(B-T) \leq 0.35$, in which case fringing fields at both edges of the line interact with each other. This results in a slightly higher characteristic impedance because the actual total capacitance to ground is less than that obtained from Figure 5.17 (which does not account for this effect). It is possible to make approximate corrections by increasing the parallel-plate capacitance (increasing W) to compensate for the loss of fringing capacitance [GETSINGER, 1962]. If an initial value W_1/B is found to be less than $0.35(1-T/B)$, a new value, W_2/B can be used where

$$W_2/B = \frac{0.07(1-(T/B)) + W_1/B}{1.20} \tag{5.8}$$

provided that $0.1 < (W_2/B)/(1-(T/B)) < 0.35$. This formula is based on a linear approximation to the exact fringing capacitance of single thin strip for a $(W/B)/(1-(T/B))$ ratio between 0.1 and 0.35.

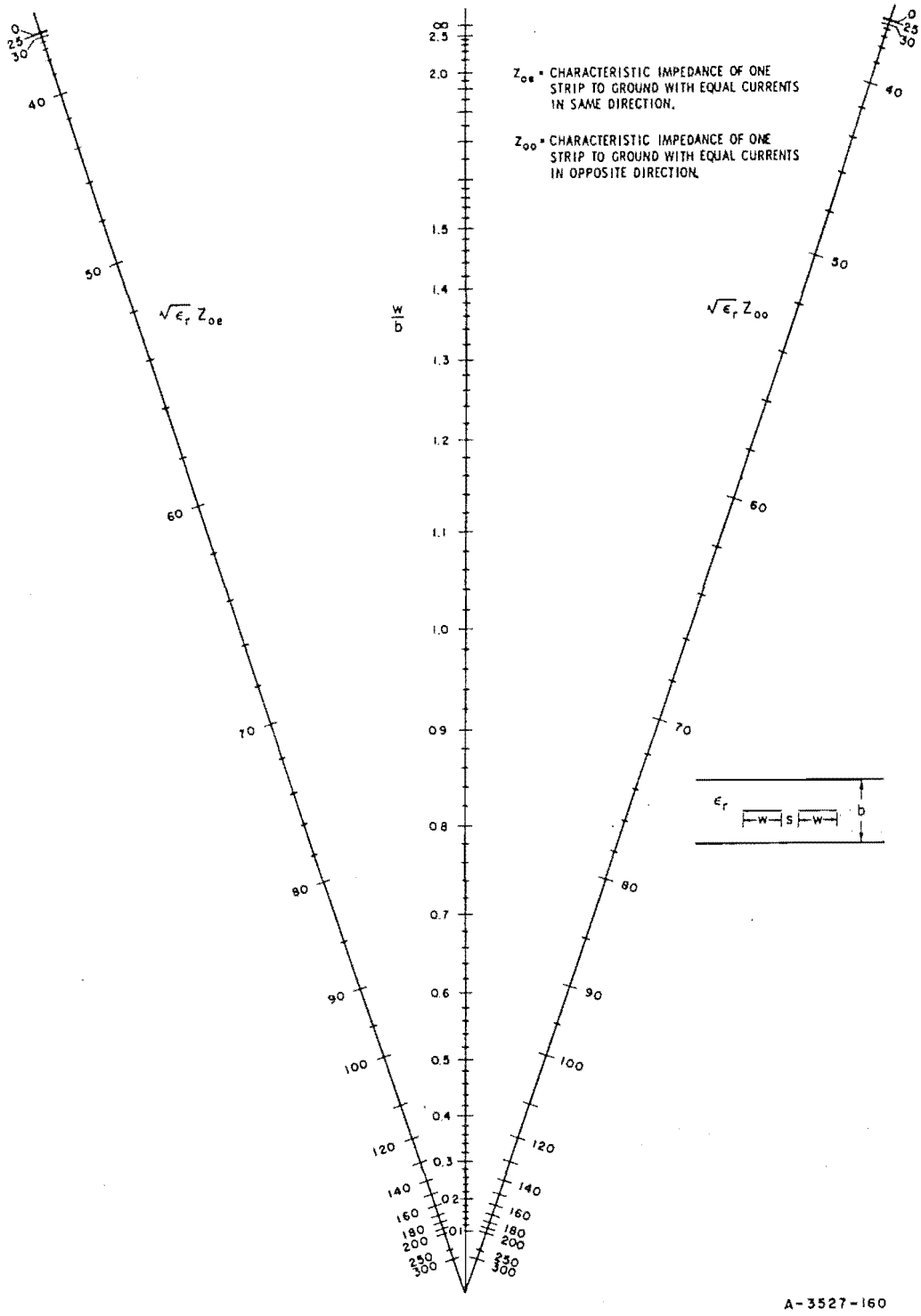


Figure 5.17 Nomogram giving W/B as a function of Z_{oe} and Z_{oo} for zero thickness strips [COHN, 1955b].

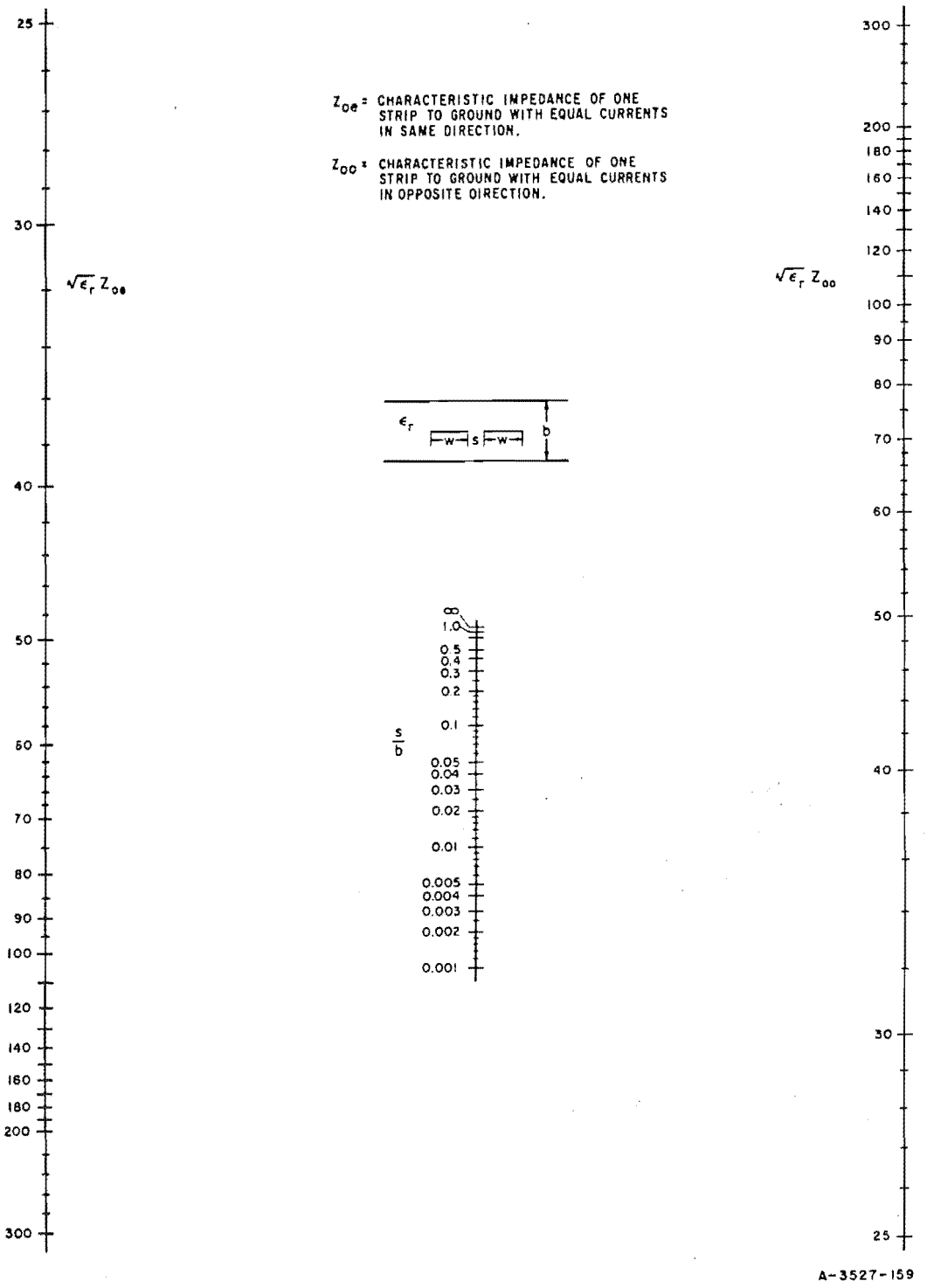


Figure 5.18 Nomogram giving S/B as a function of Z_{oe} and Z_{oo} for zero thickness strips [COHN, 1955b].

Applying equation 5.8 would give a small correction to a quantity that is reasonably close to the correct value. The resolution of the fabrication process should also be taken into account since it is not worth seeking the exact value if one cannot build it.

In the single coupler design, the author simply chose to use the next larger integer value of the design unit (*mil*) for the line width, and the nearest integer value for the spacing. These values are given in brackets in Table 5.1. Equation 5.8 was not applied because it was not known until after this prototype had been fabricated. In this case, one would expect the characteristic impedance to be higher than 50 Ω. However, this should not be too serious provided one can completely characterize all the port parameters of the couplers. The mismatch effects can then be taken into account in the FDR measurements.

The line width of the dual coupler has been corrected, and is given in Table 5.1. The values of W and S used in the actual fabrication process are given in brackets.

5.2.3.3 Single strip line width

The line width of a single strip line (non-coupled section), which should be wider than the the line width of the coupled section, may be obtained from Figure 5.19 [COHN, 1955a].

For a weak coupler, the line widths of the coupled section and the non-coupled section are approximately the same. Therefore, the values given in Table 5.1 were also used for the non-coupled strip line.

5.2.3.4 The physical length

The coupler physical length can be determined from the propagation delay of the coupler, or from the quarter-wavelength at the mid-band frequency. The propagation delay of a strip transmission line depends on the dielectric medium surrounding it, as given in equation 5.9 (ns/inch).

$$\tau_0 = 0.085\sqrt{\varepsilon_r} \tag{5.9}$$

Because alumina ($\varepsilon_r \approx 9.3$) has higher relative dielectric constant than fibre-glass epoxy ($\varepsilon_r \approx 4.7$) the physical geometry of the coupler implemented on alumina will be smaller for the same propagation delay (same frequency band). From equation 5.9 and the substrate relative dielectric constant of ALSIMAG 614 ($\varepsilon_r = 9.3$ at 1 MHz to 1 GHz), the propagation delay of the coupler was calculated to be 0.259 ns/inch. To achieve a mid-band frequency of 500 MHz (for the single coupler prototype) the coupler length must be 1.96 inch and 1 GHz (for the dual coupler prototype) the coupler length is 0.98 inch.

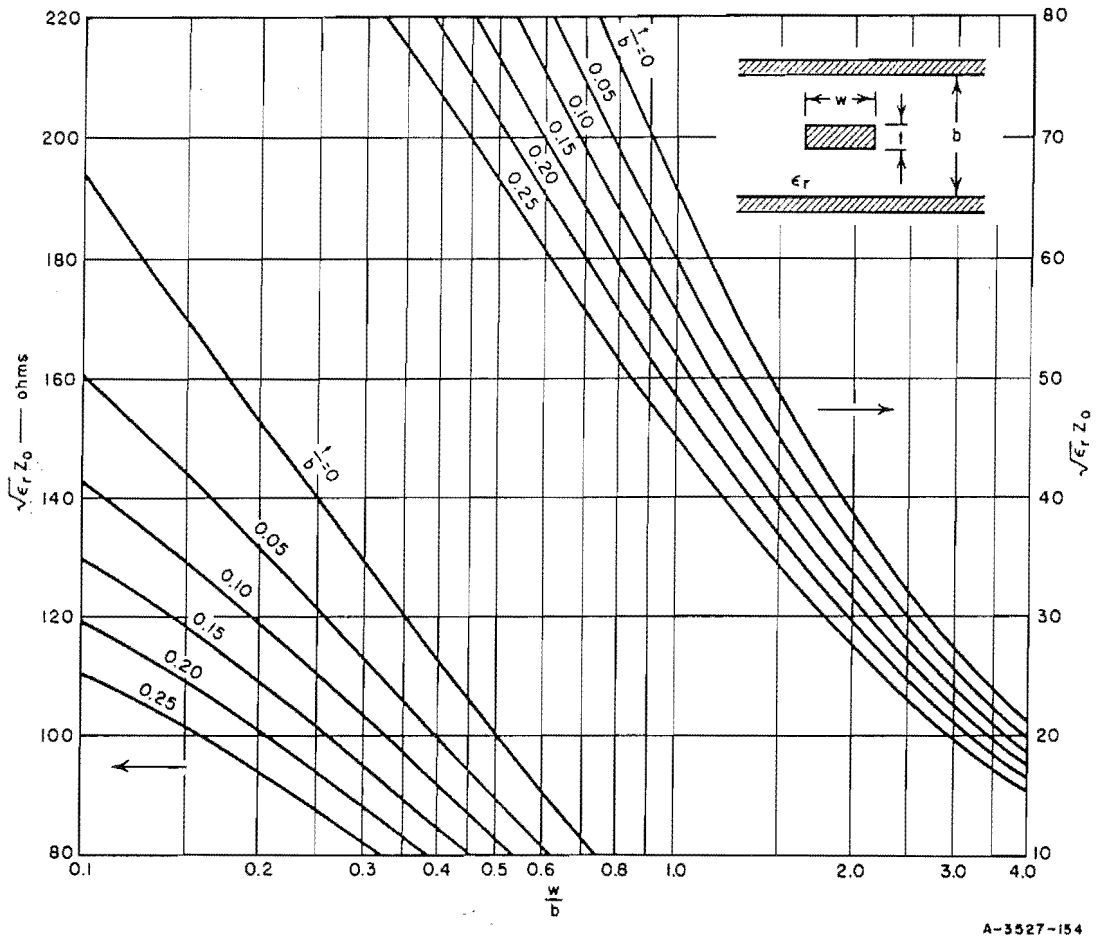


Figure 5.19 Graph giving W/B for a single strip transmission line as a function of Z_0 for various values of T/B [COHN, 1955a].

5.3 IMPLEMENTATION OF THE PROTOTYPE DIRECTIONAL COUPLERS

The Thickfilm Laboratory facility at the University of Canterbury was established between 1974 and 1978 for research and teaching purposes. The equipment and processes used here may not reflect the state-of-the-art Thickfilm technology. However, it provides aid to understanding, and fast and accessible prototype fabrication. Limitations and difficulties discussed in this thesis apply only to the processes at this laboratory, not for the technology itself.

Details of Thickfilm fabrication processes are not covered in this thesis, but are supplied as references [HARPER, 1974; HOLMES and LOASBY, 1976].

5.3.1 Layout Generation

After calculating the directional coupler parameters, the physical layout was then coded in BELLE Layout Language to generate the artwork.

After compiling and linking the BELLE code, a CIF (Caltech Intermediate Format) file describing the layout was then created by running the executable image. The BELLE and CIF codes for both prototypes are included in appendix C. Figure 5.20 shows the prototype dimensions, which correspond to the actual dimensions (in *mil*).

5.3.2 Artwork Generation

The artwork was prepared by cutting through the gelatin layer of Rubylith film using a HP7475A plotter which was loaded with a cutting tool designed specially for this purpose. The cut material was then lifted at a corner and peeled off the clear base film, leaving a copy of each ink layer obtained from the CIF files, with the clear areas corresponding to the areas to be inked.

5.3.3 Photofabrication

The artwork was cleaned to remove dust and marks that would show on the negative, and taped onto the cleaned back-lit copy board. Photoreduction of 4× master-artwork was taken using transmitted light which gives better than 500:1 contrast-ratio. Because the line width of the directional coupler is very small, to maintain the accuracy of the fabrication process four times photoreduction was used rather than the normal ten times used in the standard Thickfilm circuit process. After the film had been developed it was then used to make the printing screen.

5.3.4 The Screen Making and Printing Process

The object is to apply a sensitised coating to a mesh screen, expose the screen to ultraviolet light through the photographic negative, and produce a screen with open areas for the ink to flow through to give the desired print. The screen mesh is made from polyester. A mesh count (the number of open spaces per lineal inch) of 330 was used for printing conductors, and 196 for resistors.

5.3.5 Substrate Drying and Firing

Directly after printing the substrate was placed in a dust-free environment to allow the print to settle. The screen mesh tends to leave a pattern on the surface which will smooth out after 5 to 20 minutes, depending on the viscosity of the printed material. To make the resulting film tough enough for handling or subsequent printing the substrates must be dried. In this process only volatile organic solvents are evaporated, leaving the binders.

The firing of Thickfilm circuits is a complex process which involves several different phases. Firstly, the organic binders and solvents burn out in the neighbourhood of 500 °C, then the metallic elements develop the required characteristics at about 850 °C. Simultaneously, there is a sintering action of the colloidal glass and metal materials to

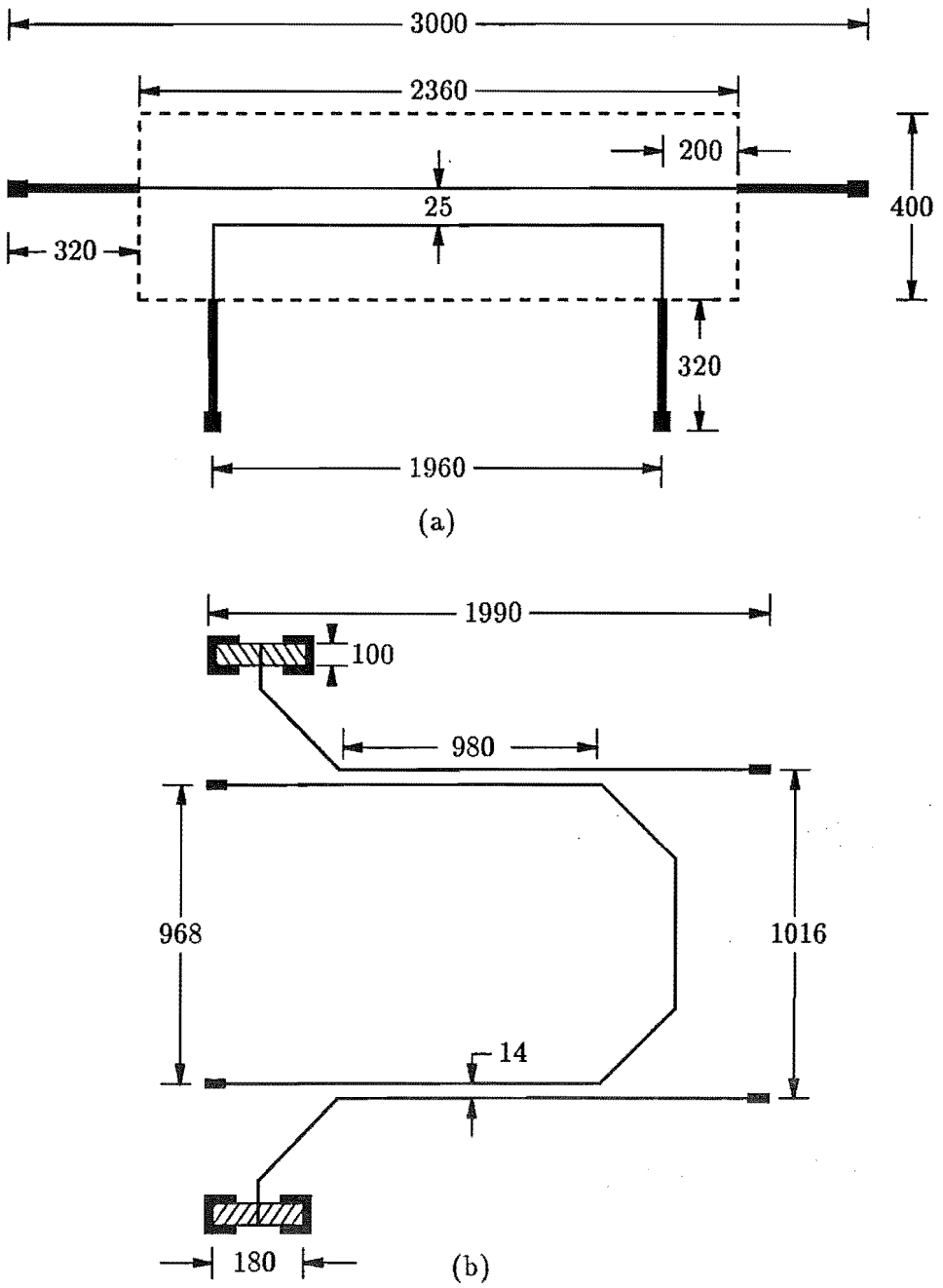


Figure 5.20 Dimensions of the prototype couplers (a) the single directional coupler (b) the dual directional coupler.

	Trade no.	Material	Resistivity (thickness = 10-15 μm)
Conductor 1	ESL 9990	Pure silver	0.0015-0.003 Ω/square
Conductor 2	ESL 9635B	Silver/Palladium alloy	0.2-0.4 Ω/square
Resistor	ESL 3912	Ruthenium-based	100 Ω/square

Table 5.2 Materials used to fabricate the prototype directional couplers.

anchor the film to the substrate and to protect the metallic elements. Hence, to obtain good reproducibility the firing process requires accurate control of both temperature and time. A continuous belt furnace with several independent temperature controlled zones is used for this purpose.

5.3.6 Resistor Trimming Process

Resistors may be adjusted in a variety of ways. Refiring produces resistance changes which may be predictable in closely controlled situations. However the most conventional means are laser and air-abrasive methods which increase resistance. There is an air-abrasive system available in our laboratory but in our case only two resistors need to be trimmed so we used a diamond burr driven by a Kool-Torque air-motor running as high as 55,000 RPM to gradually remove resistor material until the proper value was reached (through TDR measurement).

5.3.7 Materials

The materials, and some important data used in this experiment, are listed in Table 5.2. For full details of these materials, the readers are refered to Electro-Science Laboratory (ESL) data-sheets.

Only conductor and resistor pastes were required. Silver paste (ESL 9990) was used to print conductors because of its higher conductivity, but its solder leach resistance is poor so silver-palladium paste (ESL 9635B) was used to print the pads and ground plane. Ruthenium-based resistor paste (ESL 3912) was used to produce nominally 50-ohm internal termination resistors for the dual directional coupler.

5.4 THE PHYSICAL STRUCTURE

Both couplers were constructed using the tri-plate configuration shown in Figure 5.21 (a). The screen printing process cannot give a square conductor cross sections, but produces the cross section shown in Figure 5.21 (b).

To prevent silver migration and fill the air gap, a silicone gel (ε_r = 2.95) was used (Figure 5.21 (b)). Alumina powder filled silicone would more closely match the

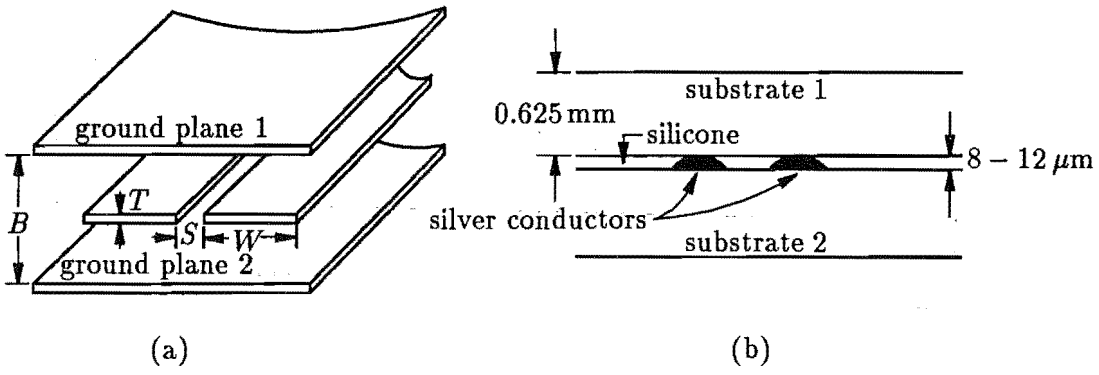


Figure 5.21 The prototype implemented in tri-plate configuration (a) basic structure (b) actual cross section.

substrate dielectric constant ($\varepsilon_r = 9.3$), but the air-gap, at 9 μm, is not troublesome.

The two prototypes were packaged in two entirely different styles. These packages were designed for testing purposes during development and will not be used in the final implementation. Detailed design of these two packages will next be presented.

5.4.1 The Single Directional Coupler

From Figure 5.20 (a), there are five transmission line sections. The first is a 50 Ω microstrip line 240 *mil* long; the second is a single strip line 200 *mil* long; the third is the directional coupler which is 1960 *mil* long; the fourth is a single strip line 200 *mil* long; the last is a 50 Ω microstrip line 240 *mil* long. The soldering pads for the microstrip lines are 80 *mil* $\times$ 80 *mil*.

The ground planes are interconnected by soldering 1.28 mm by 0.8 mm diameter copper pins through CO_2 laser drilled holes, shown in Figure 5.22.

Microstrip transmission line was used to connect the coupler to the measurement circuit which, in the final phase, will be included on the same substrate. The top ground plane was designed to cover only the coupler section and the strip lines, so as to ensure that only one TEM propagation mode is present.

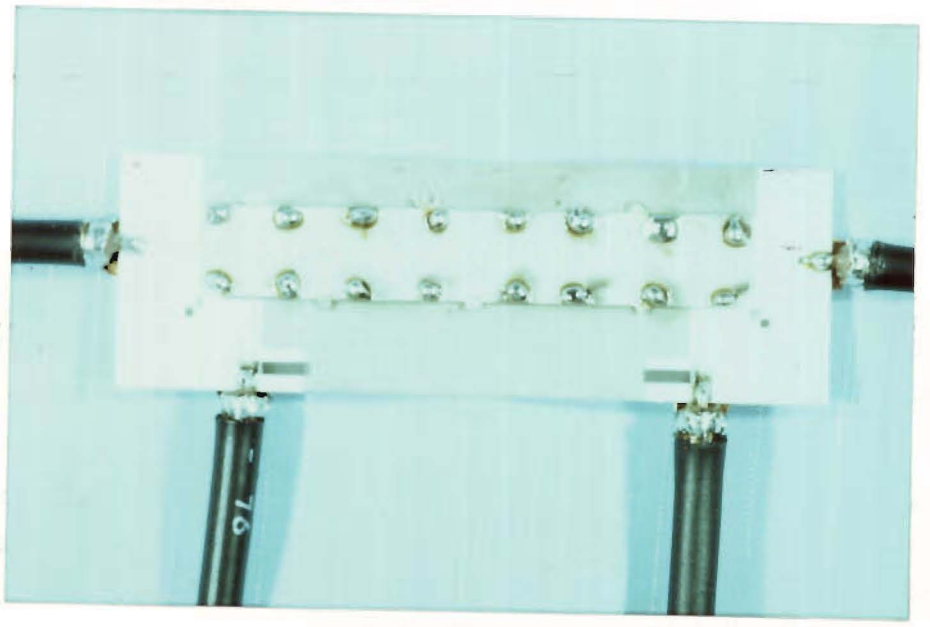
The equation used to calculate the microstrip line width (for narrow strips, $Z_0 > 44 - 2\varepsilon_r$) is [EDWARDS, 1981]

$$W/H = \left(\frac{e^{\acute{H}}}{8} - \frac{1}{4e^{\acute{H}}}\right)^{-1} \tag{5.10}$$

where

$$\acute{H} = \frac{Z_0\sqrt{2(\varepsilon_r+1)}}{119.9} + \frac{(\varepsilon_r-1)}{2(\varepsilon_r+1)}\left(\ln(\pi/2) + \frac{1}{\varepsilon_r}\ln(4/\pi)\right) \tag{5.11}$$

The line width was computed to be 0.641 mm or 25.2 *mil* and 25 *mil* was used in the actual implementation.



(a)

(b)

Figure 5.22 Photographs of the single coupler (a) front (b) back.

For testing purposes, the prototype coupler was connected to 50 Ω coaxial cables (ASC-URM-76) and then to BNC connectors, as shown in Figure 5.22, using Multicore SN62 (62/36/2:Sn/Pb/Ag) solder.

5.4.2 The Dual Directional Coupler

To minimize discontinuties, there is no microstrip line in this coupler (Figure 5.20 (b)) and 45-degree turns are used instead of abrupt 90-degree turns. The arrangement of this circuit was designed to be symmetrical so that the outputs from ports 3 and 4 can easily connect to the detector circuits.

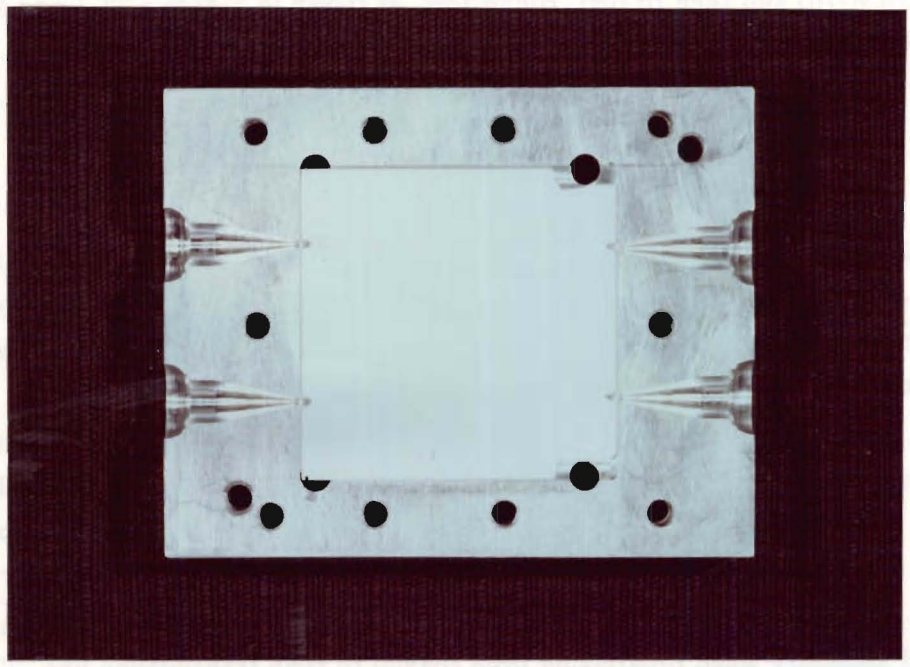
The author decided to use type-N instead of BNC connectors to facilitate interfacing with the automatic network analyzer. Two aluminium plates, each 0.5 inch thick, were used to house the coupler. Figure 5.23 shows the packaging of this second prototype.

The dimensions of the transition from a type-N connector to a solder pad of the coupler are given in Figure 5.24 (a). The transition was designed to match both impedance and field geometry when progressing from coaxial to strip transmission line. The outer and inner conductors of the coaxial line were tapered to maintain the characteristic impedance constant at 50 Ω. The outer conductor diameter was linearly reduced to match the ground plane spacing (B) of the strip line, and should provide a smooth transition of field pattern from coaxial to strip line. Figure 5.24 (b) is a photograph of the transition region. The copper wire of 0.5 mm diameter was used to reduce mechanical stress at the strip-line connection. The wire diameter was later changed to 0.29 mm since the first one was too solid. The soldering pads are $30\,mil \times 50\,mil$.

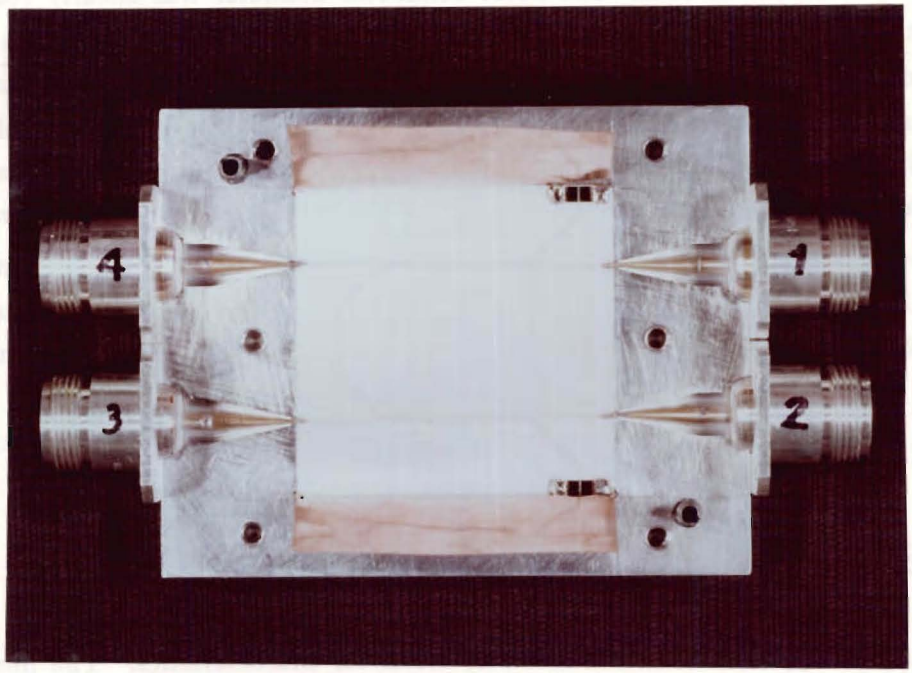
Silicone was applied between the two substrates. To achieve good ground plane conductivity, two copper sheets were placed between the substrates and the aluminium bars. This was later changed because of difficulty in maintaining constant ground plane spacing leading to fluctuating characteristic impedance along the strip lines. Instead of using copper sheet, the ground plane was printed on the back of both substrates.

5.5 COUPLER TEST RESULTS

The two prototypes were tested for their electrical characteristics. The line width and spacing, which determine the characteristic impedance and coupling factor, were measured using a microscope. Characteristic impedance can be approximated by using TDR, but the most important data are their S-parameters, which must be accurately determined. An automatic network analyzer (ANA) is required for such measurements. Unfortunately, there is no ANA at the University of Canterbury, so the prototypes were sent to the Department of Electrical & Electronic Engineering, University of Auckland, where the measurements were performed.

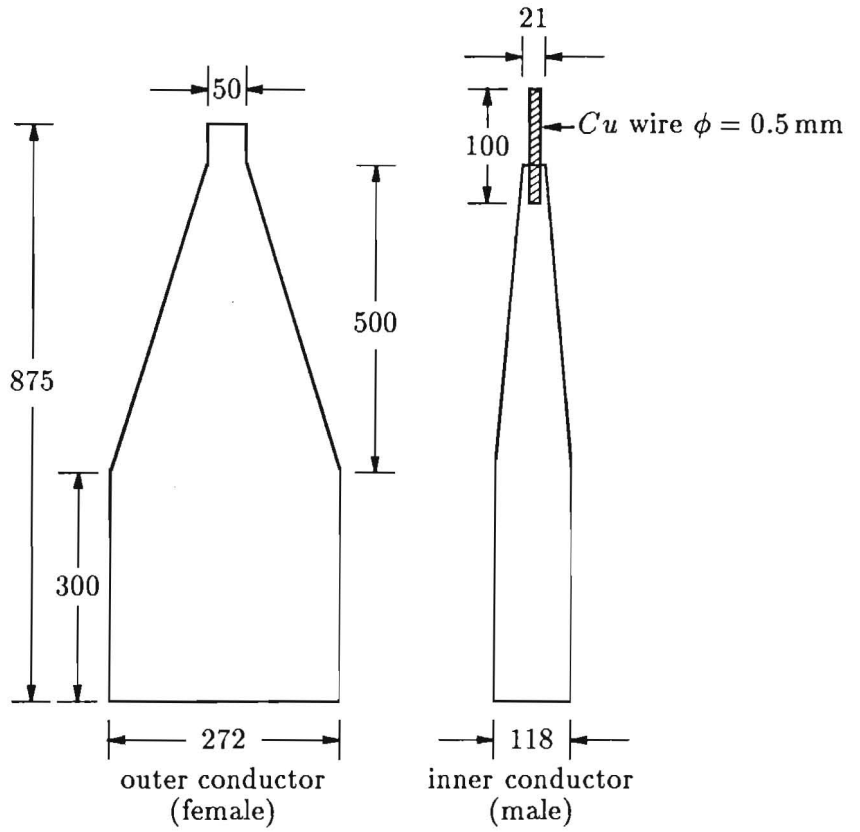


(a)

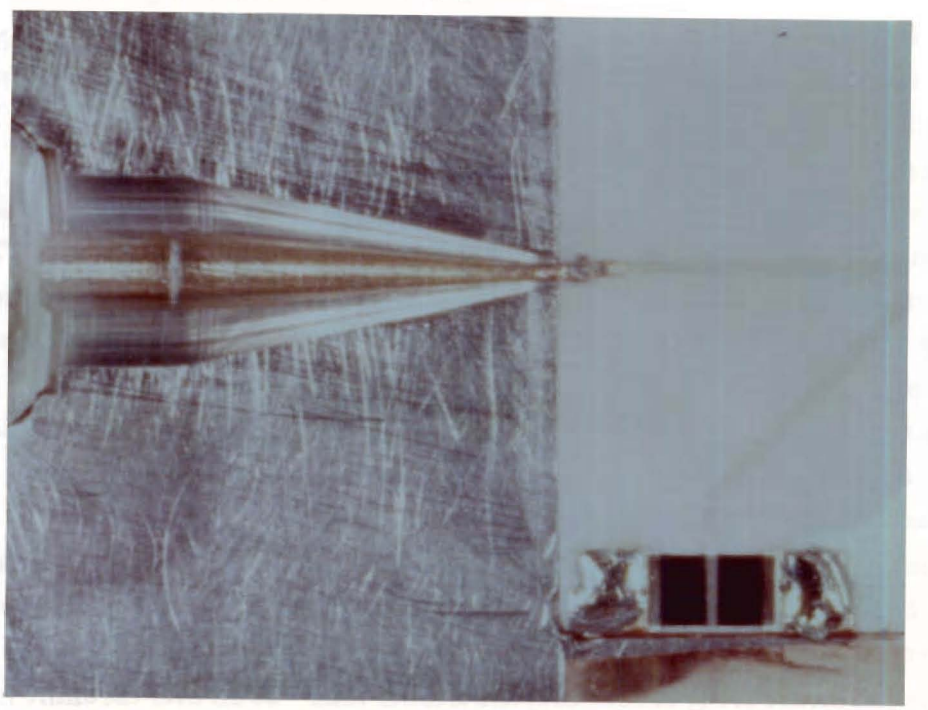


(b)

Figure 5.23 Illustrating the packaging of the dual directional coupler (a) top, with the substrate in place (b) bottom, with the substrate in place, in which connections have been made to the coaxial-stripline transitions.



(a)



(b)

Figure 5.24 (a) Illustrating the transition from a type-N connector to a solder pad of the strip transmission line (b) photograph of the transition.

	Width (W)	Spacing (S)
Single coupler	0.264 mm (10.4 *mil*)	0.633 mm (24.9 *mil*)
Dual coupler	0.314 mm (12.4 *mil*)	0.352 mm (13.9 *mil*)

Table 5.3 Measured parameters for the prototype directional couplers.

5.5.1 Coupler Line Width and Spacing Measurement

The conductor line widths and spacings of the two prototypes were measured using a light-section microscope, and are presented in Table 5.3. These values were measured to ensure that the critical parameters are within an acceptable tolerance. The fabrication process can be tightly controlled to obtain the desired values of these parameters, but that is not critical at this stage.

5.5.2 Directional Coupler S-parameters

To characterize the prototype directional couplers the necessary four port S-parameters were measured using a HP8510 Automatic Network Analyzer over a frequency range from 100 MHz to 1 GHz at 20 MHz intervals. Only S_{21}, S_{31}, and S_{41}, which are of prime interest, are plotted in Figures 5.25 to 5.27. The remaining results are given in appendix D. The ANA was calibrated to the connector planes of the prototypes, not to the input and output ports of the couplers. Therefore, these S-parameters represent the entire package rather than the actual coupler.

The magnitude of the transmission factor (S_{21}) indicates that the TFH couplers have relatively high conductor losses, but dielectric losses are negligibly small at this frequency range (Dissipation Factor of Alumina, $D = \tan\delta \leq 0.0003$). The silver conductors exhibit higher resistivity than pure silver. Because the conductors taper to thin irregular edges, these regions of high current flow coincide with relatively high edge resistivity and hence undesirably high I^2R losses.

Better fabrication techniques, such as etching overwidth conductors to thicken the edges, or direct lithography (not screen printing) methods can be used to realise a near-rectangular conductor cross section.

The measured S_{31} of both prototypes agrees with the theoretical responses (equation 5.2). The deviation from theoretically computed values is more likely to be caused by interface imperfections than coupler fabrication error.

The magnitude of S_{41} of both couplers is lower than -32 dB over the entire frequency range. The directivity (S_{41}/S_{31}) of the dual coupler is better than that of the single coupler, especially at frequencies above 500 MHz. This is because of differences in the structure of the coupler, and because the coupling factor of the dual coupler is twice that of the single coupler, yielding lower value of the ratio S_{41}/S_{31}.

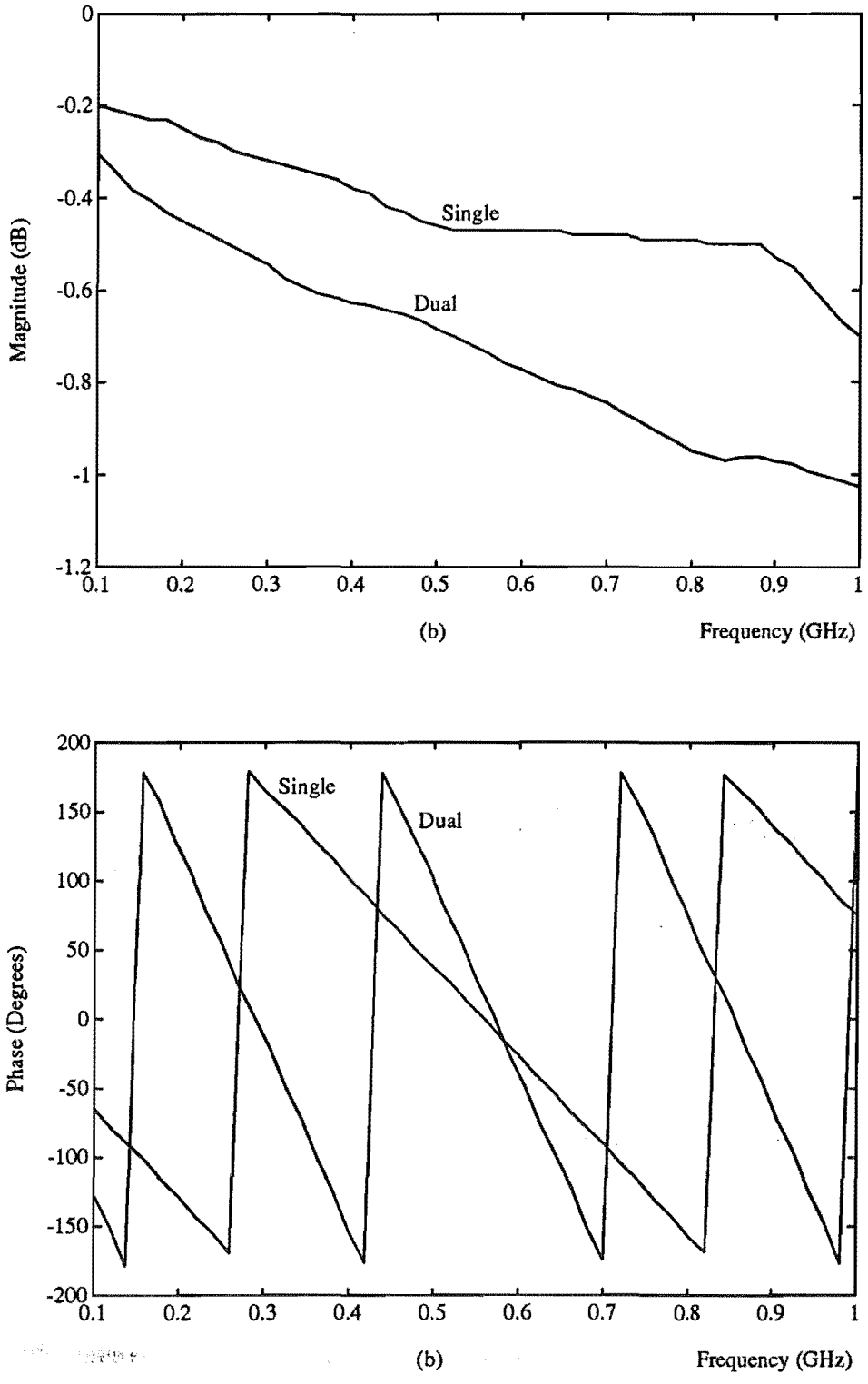


Figure 5.25 Measured S_{21} of the prototype couplers (a) magnitude (b) phase.

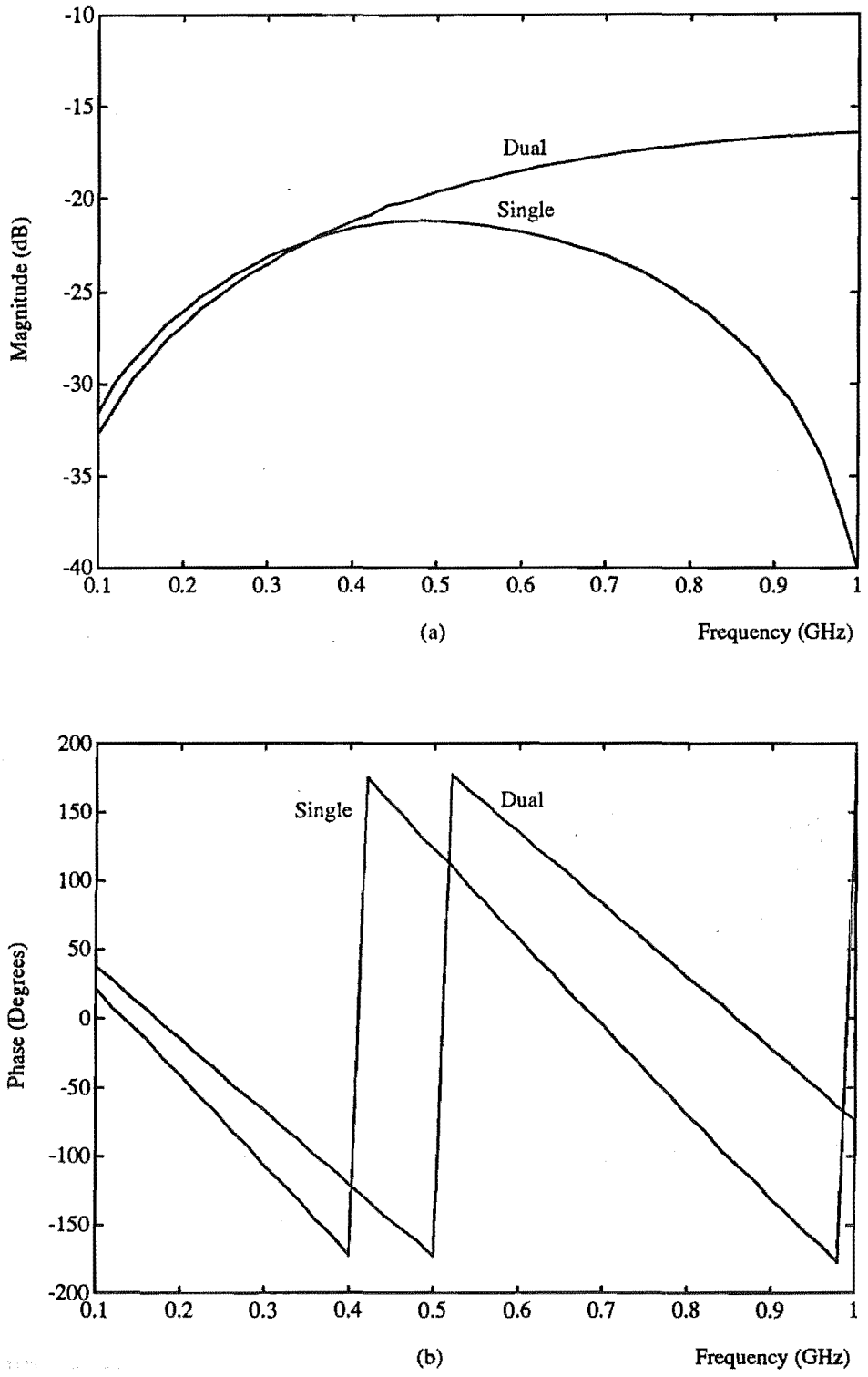


Figure 5.26 Measured S_{31} of the prototype couplers (a) magnitude (b) phase.

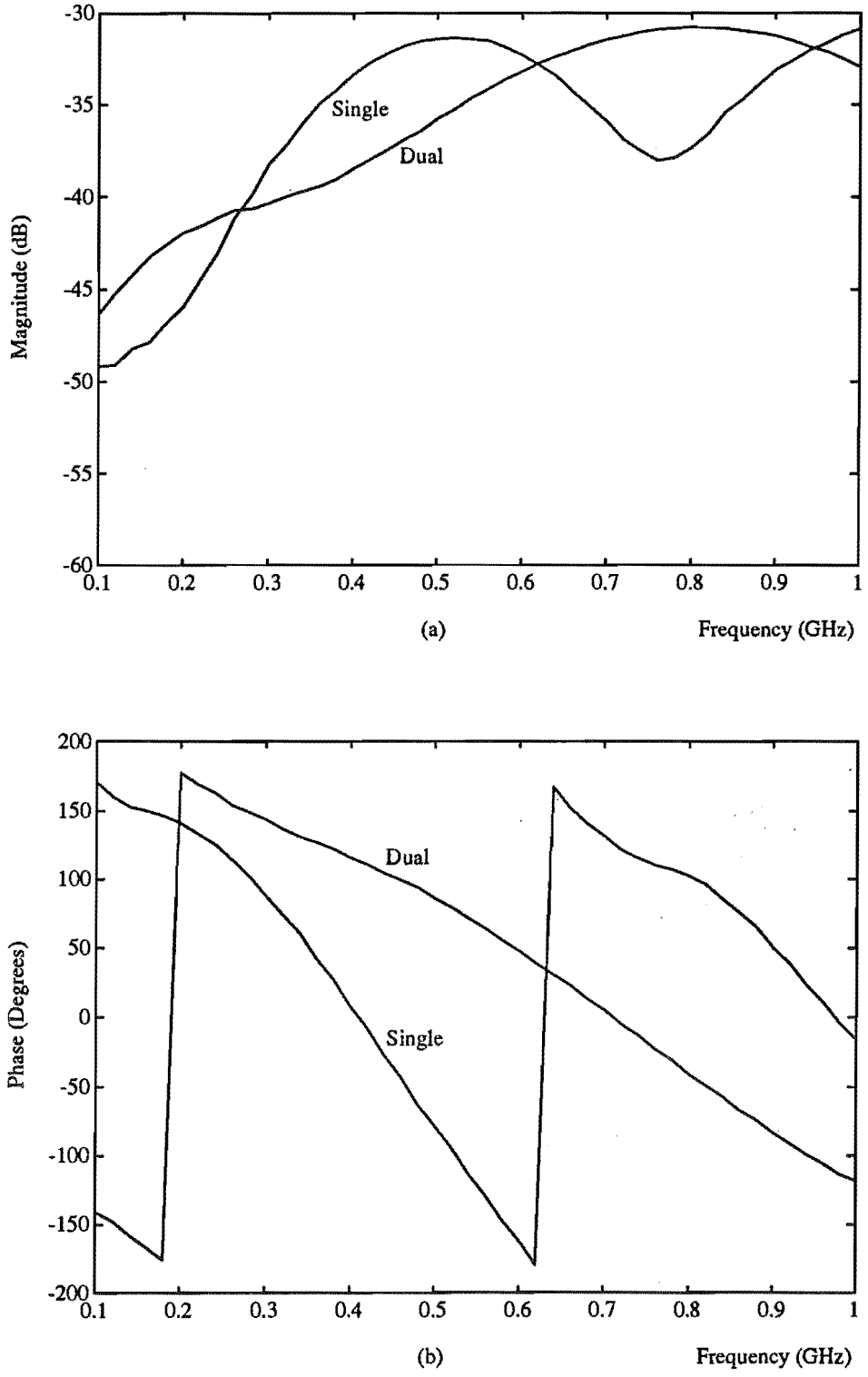


Figure 5.27 Measured S_{41} of the prototype couplers (a) magnitude (b) phase.

By comparison with a HP 778D Dual Directional Coupler, the prototype directional couplers have considerably higher reflection coefficients at all four ports. This is chiefly because the coupler characteristic impedance is higher than the required $50\,\Omega$, and partly due to the imperfect interfaces. The reflections caused by impedance mismatches can be reduced by experimenting with different line widths. However, due to the inaccessibility of the network analyzer needed to measure the S-parameters, further investigation in this direction was not pursued.

5.6 CONCLUSION

This chapter has briefly introduced the theory of electromagnetic coupling between parallel-coupled lines. The application of directional couplers to separately determine incident and reflected waves has been investigated. The directional coupler responses both in steady state and transient were presented, including application to the timing alignment of PEC outputs.

Two prototype directional couplers were designed and implemented to study the feasibility of the proposed system as described in the previous chapter. The prototype design and fabrication processes were also presented, together with a brief review on the Thickfilm process.

Measurement results reveal that a directional coupler fabricated using TFH technology is feasible, and is small enough to be included in every PEC. The coupler performance is not a major design requirement, provided that it can be fully characterized. Reflections, caused by impedance mismatches between the coupler ports and the hybrid-transformer/peak detector circuitry (or its functional equivalent) foreshadowed in Figure 3.3, will reduce the accuracy of the FDR measurement, and must be minimized.

CHAPTER 6

THE FDR EXPERIMENT

To further investigate the performance of the prototype couplers, FDR experiments were carried out over the frequency range from 100 MHz to 1 GHz, at 100 MHz intervals. FDR measurement results using the prototype couplers are compared with the results of those using a HP 778D Dual Directional Coupler and those from a HP8510 Automatic Network Analyzer. The HP778D, as a *known good* directional coupler, is used to verify the measurement technique.

Section 6.1 describes the objective and details the terminations used as known loads in this experiment. The measurement configuration and results are presented in sections 6.2 and 6.3. Section 6.4 discusses the results and some problems which were encountered during the experiment.

6.1 OBJECTIVES

The aim of this experiment is to investigate the performance of the prototype directional couplers and the practical accuracy to be expected from this technique. Results are presented for three sets of load terminations; capacitive, inductive, and resistive loads. Although a sliding short circuit would provide the best known reactive load, it is difficult to construct, especially for low frequency measurements. Validation of the measurement principle is based on results from the HP778D Dual Directional Coupler used as a reference standard.

6.1.1 The Construction of the Terminations

Figure 6.1 shows all the BNC connectors terminated with the loads used in the FDR experiments. These loads were characterized over the frequency range of interest using an ANA.

The capacitive loads employ Vitramon 0805 NPO $\pm 0.5\,\mathrm{pF}$ ($< 10\,\mathrm{pF}$) and $\pm 5\%$ ($\geq 10\,\mathrm{pF}$) tolerance chip capacitors. The insulator (PTFE) between the outer conductor and the inner conductor of the BNC connector was cut to a suitable shape and size to imbed the chip capacitors ($80\,mil \times 50\,mil$). Their nominal and measured (ANA)

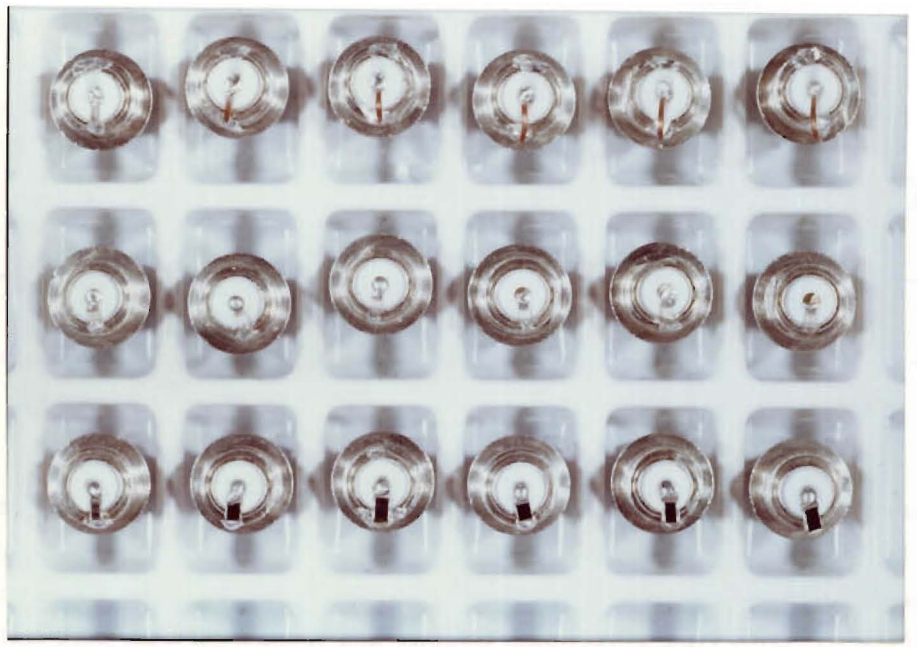


Figure 6.1 Photographs of BNC connectors mounted with the loads for the FDR experiment; the top row shows the inductive loads; the middle row shows the capacitive loads; and the bottom row shows the resistive loads.

values are given in Table 6.1.

The inductive loads were made of 0.8 mm diameter copper wire cut to different lengths and soldered to BNC connectors in the same way as the capacitive loads. The inductor values (in nH) were calculated based on the inductance of a straight wire, as given by [TERMAN, 1943]

$$L = 0.2\ell[\ln(2\ell/R) - 0.75] \tag{6.1}$$

where R is the wire radius and ℓ is the wire length, both values are in mm. In this case the diameter of the wire (without insulation) was measured at 0.69 mm. Instead of designing for a particular value of inductor, the wire was cut to appropriate lengths, 2, 4, 6, 8, 10, and 12 mm. Their estimated and measured (ANA) inductances are listed in Table 6.1.

The resistive loads were chosen from some surplus Thickfilm substrates. Resistors having the desired values and size were then cut out and mounted on BNC connectors in similar manner to the capacitive and inductive loads. The measured *d.c.* and ANA (derived) values of these resistors are given in Table 6.1.

6.2 MEASUREMENT CONFIGURATION

Using the configuration of Figure 6.2 (a), and a HP 8405A Vector Voltmeter, the magnitude and phase of the coupled incident and reflected waves were measured at

Load	Capacitive loads		Inductive loads		Resistive loads	
	Nominal	ANA	Estimated	ANA	*d.c.*	ANA
1	1 pF	$0.31 - j379.6$	0.68 nH	$0.06 + j2.7$	4.4 Ω	$4.26 + j5.9$
2	2.2 pF	$0.39 - j176.8$	1.92 nH	$0.08 + j3.8$	46 Ω	$44.6 + j5.9$
3	4.7 pF	$0.51 - j59.5$	3.37 nH	$0.05 + j8.7$	146 Ω	$142.1 + j12.8$
4	8.2 pF	$0.42 - j36.3$	4.95 nH	$0.04 + j9.9$	444 Ω	$432.1 + j53.7$
5	18 pF	$0.37 - j15.3$	6.63 nH	$0.02 + j14.3$	702 Ω	$672.7 + j134.6$
6	33 pF	$0.26 - j6.1$	8.4 nH	$0.01 + j19.3$	1.49 kΩ	$1307 + j535.8$

Table 6.1 List of the capacitive, inductive, and resistive terminations, used in the FDR experiment. ANA results are given as $Z_L = R_L + jX_L$ (Ω) at 500 MHz.

ports 3 and 4 of the directional coupler. An ANA measurement topology is similar to this configuration, with the difference that an ANA employs more sophisticated measuring circuits and includes automatic calibration and error correction.

The SFG in Figure 6.2 (b) applies to the dual directional coupler where the interaction between ports 3 and 4 is negligibly small ($S_{34} = S_{43} \approx 0$). S_{AD} represents the two-port S-parameters of the connectors required to connect the load to port 2 of the directional coupler.

The SFG in Figure 6.2 (c) is simplified from Figure 6.2 (b), assuming perfect matches at ports 3 and 4 (i e. $\Gamma_{DA} = \Gamma_{DB} = 0$).

6.2.1 Relative Reflection Coefficient Measurement

Problems occur in this experiment because the adaptors affect the measurement accuracy. To achieve accurate results, one should really measure the connector S-parameters and include them in the flow graph of the measurement configuration.

Our particular equipment configuration requires two successive adaptors to connect a female BNC termination to a female type-N connector. Because their S-parameters are not available, we assume them to be perfectly matched ($S_{11}^{AD} = S_{22}^{AD} = 0$), and therefore appear merely as an extra length of transmission line between the coupler (port 2) and the load. The extra time delay may be analytically derived from their physical lengths and construction, or by measurement. The relative measurement technique, described in this section, is an alternative method of obtaining magnitude and phase readings.

With these assumptions, the SFG in Figure 6.2 (c) can be further reduced as shown in Figure 6.3.

These simplifications allow one to measure all the loads with respect to a reference load; for example a short or open circuit may be used. In this method the phase reading

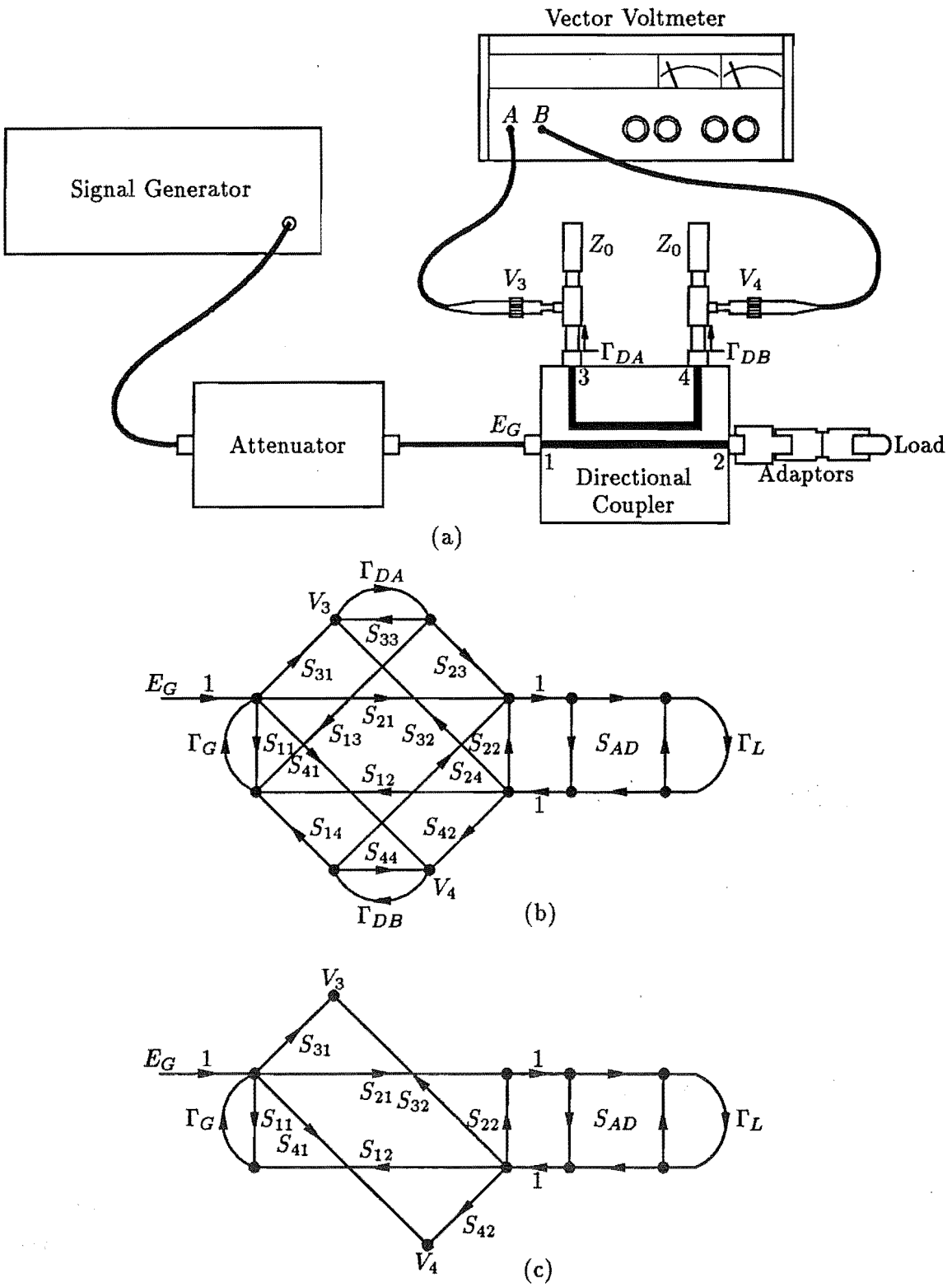


Figure 6.2 The FDR experiment configuration (a) circuit diagram (b) its complete flow graph (c) flow graph obtained by assuming perfect matches at the detectors.

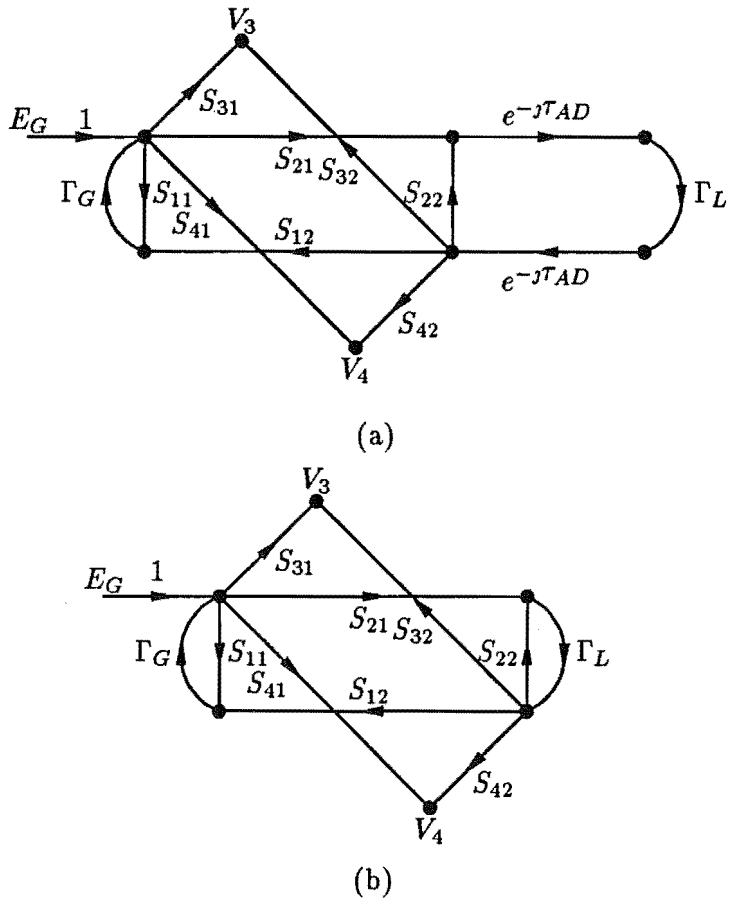


Figure 6.3 Simplified SFG (a) assuming perfect connector (b) SFG used in the relative reflection coefficient measurement.

is taken to be the difference between the indicated and the reference phase readings, because the phase delays caused by the adaptors cancel out. This leads to the SFG shown in Figure 6.3 (b), where the adaptor S-parameters are omitted. This SFG will be used in the computation of the load reflection coefficients Γ_L from the measured voltages at ports 3 and 4 of the directional coupler.

The major advantage of relative measurement is that its accuracy is relatively better than an absolute measurement, because the effects of coupler imperfection (such as coupler tracking and directivity) are balanced out in the reading. The disadvantage is that all elements in the measurement configuration, including the references (s/c and o/c) must be accurately characterized. The relative measurement accuracy depends upon how accurately these elements can be determined, and the incremental accuracy of the measuring equipment.

Although this method minimizes the adaptor problem, unavoidable instrument inaccuracy still remains. The best one can expect is to obtain results with errors within the specification of the instrument and this is the goal to be achieved here.

6.2.2 The Reference Loads

Both open circuit and short circuit reference loads were employed, and they were characterized for their reflection coefficient over the frequency range of 100 MHz to 1 GHz using the HP 8510 ANA. A photograph and S_{11} for these loads are shown in Figure 6.4 (a) and (b) respectively.

To obtain the best phase accuracy from the vector voltmeter, each load was measured with respect to a selected reference (short or open circuit) whichever was closer to the phase reading for that load. Such an inconvenient procedure arose because the accuracy required in this application approaches the accuracy specifications of the HP8405A Vector Voltmeter (designed in 1966). With 1991 technology the author expects that in the final implementation of this system, only a short circuit (which gives a nearly ideal reference over the frequency range of interest) will be required.

6.2.3 Output Voltages at Ports 3 and 4

From the SFG in Figure 6.3 (b), assuming $\Gamma_G = 0$, the voltage at port 3 of the coupler is

$$\frac{V_3}{V_1} = \frac{S_{31}(1 - S_{22}\Gamma_L) + S_{21}S_{32}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{6.2}$$

and the voltage at port 4 is

$$\frac{V_4}{V_1} = \frac{S_{41}(1 - S_{22}\Gamma_L) + S_{21}S_{42}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{6.3}$$

From the above two equations, one may predict the phase reading of each load from the ratio V_4/V_3, obtained by substituting the value of the corresponding Γ_L (which was measured with the ANA) into equation 6.4.

$$\frac{V_4}{V_3} = \frac{S_{41}(1 - S_{22}\Gamma_L) + S_{21}S_{42}\Gamma_L}{S_{31}(1 - S_{22}\Gamma_L) + S_{21}S_{32}\Gamma_L} \tag{6.4}$$

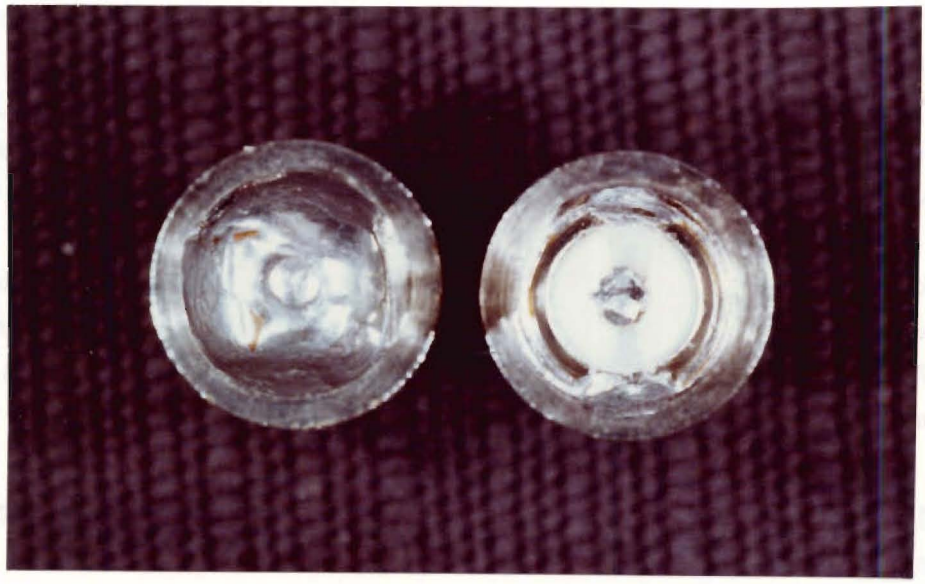
For example: for an ideal coupler ($S_{11} = S_{22} = S_{32} = S_{41} = 0$), equation 6.4 becomes simply $\frac{V_4}{V_3} = \frac{S_{21}S_{42}\Gamma_L}{S_{31}}$.

In normal operation, one would compute Γ_L from the complex ratio of the reflected to the incident waves (V_4/V_3). The equation used to obtain the reflection coefficient Γ_L from the measurement values is (derived from equation 6.4)

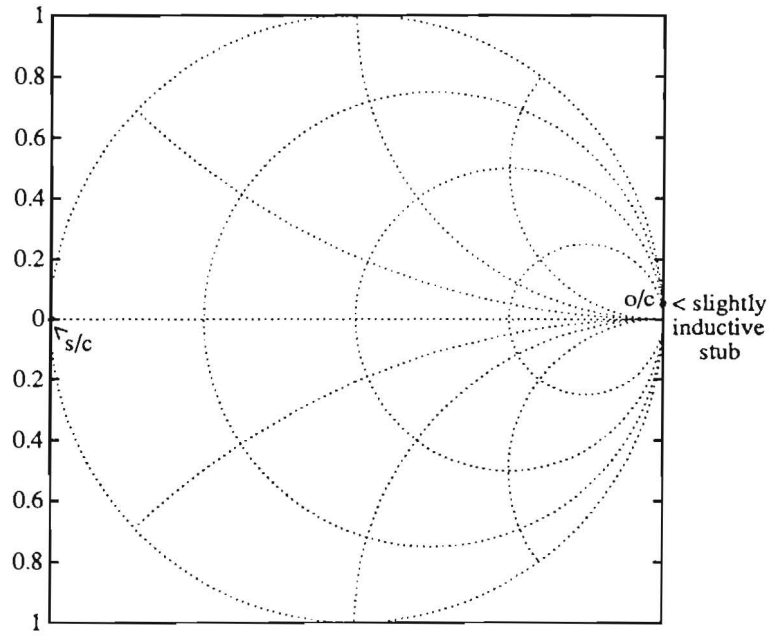
$$\Gamma_L = \frac{S_{41} - (V_4/V_3)S_{31}}{S_{22}S_{41} - S_{21}S_{42} + (V_4/V_3)(S_{21}S_{32} - S_{22}S_{31})} \tag{6.5}$$

6.3 MEASUREMENT RESULTS

The reflection coefficients of all the loads were obtained from the measured voltages at ports 3 and 4, using equation 6.5. These results indicate that the simplification arrived at in Figure 6.2 (c) is effective *only* when the coupler is lossless, matched,



(a)



(b)

Figure 6.4 Reference loads for the FDR experiment (a) photograph of short and open circuits (b) S_{11} the reference loads.

and has high directivity. When the detector reflection coefficients Γ_{DA} and Γ_{DB} are assumed to be zero, some finite coupler parameters, $S_{13}, S_{23}, S_{33}, S_{14}, S_{24}$, and S_{44}, disappear. Such an assumption is acceptable for the HP778D which has high directivity

and a characteristic impedance close to 50 Ω, but is presently unsuitable for the sub-optimal TFH prototypes. Further TFH coupler development is expected to improve this situation.

The reflection coefficient of the probe tee (terminated with a 50 Ω load) must be measured with the vector voltmeter probe in its position. The author has been unable to do this because the ANA is at the University of Auckland but the vector voltmeter is at the University of Canterbury.

For the above reasons, the prototype results (which are outside specification bounds of the measuring equipment) are not included here but are given in appendix E. The HP778D results, which are comparable to the results obtained from the ANA, are next presented.

6.3.1 The HP778D Dual Directional Coupler Load Measurement Results

These results are presented in comparison with those much more accurate results obtained using the HP8510 ANA. The reflection coefficients are presented as Smith charts. The solid line is the result from the HP 8510 ANA; the dashed line is the the HP 778D dual directional coupler result.

Plots for capacitive, inductive, and resistive loads appear in Figures 6.5 to 6.7, Figures 6.8 to 6.10, and Figures 6.11 to 6.13 respectively.

6.4 DISCUSSION OF THE RESULTS

In this section, measurement errors and their effects on the FDR results are examined.

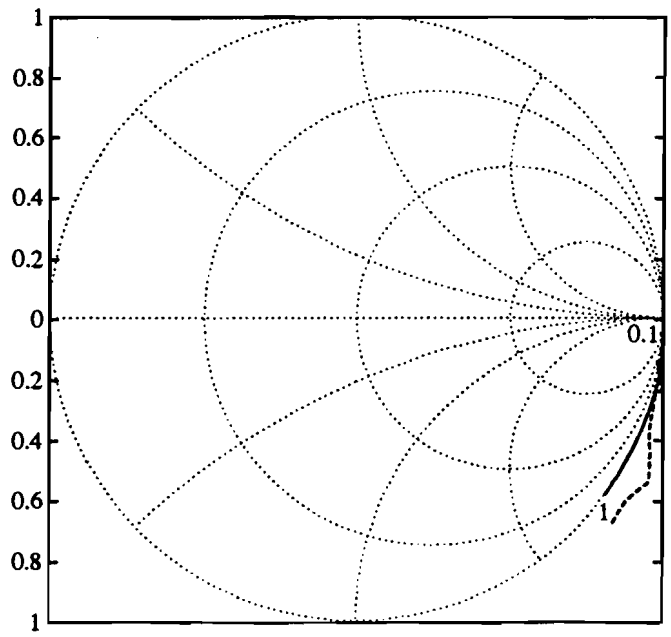
To evaluate the practical accuracy of this technique, we plot the differences between the HP778D and the reference (ANA) results. Comparison of both magnitude and phase is made only at 100, 500, and 900 MHz, since these frequencies represent typical low-band, mid-band, and high-band frequencies.

6.4.1 Measurement Error Sources

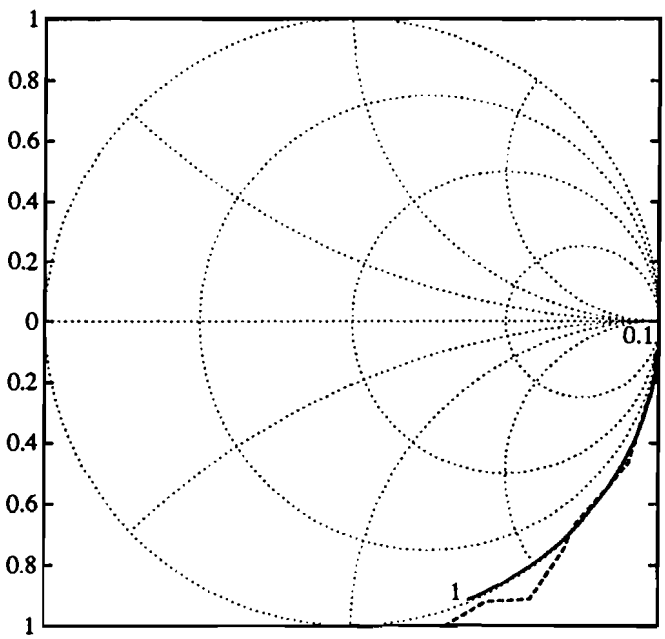
The major sources of measurement error are:

1. Impedance mismatch

   This is believed to be the major contribution to experimental error. Reflections from the detectors, Γ_{DA} and Γ_{DB}, are likely to be the main contributors. Although these values are close to zero, they cannot be assumed zero for a mismatched coupler, especially if the mismatches are at ports 3 and 4 (S_{33} and $S_{44} \neq 0$).

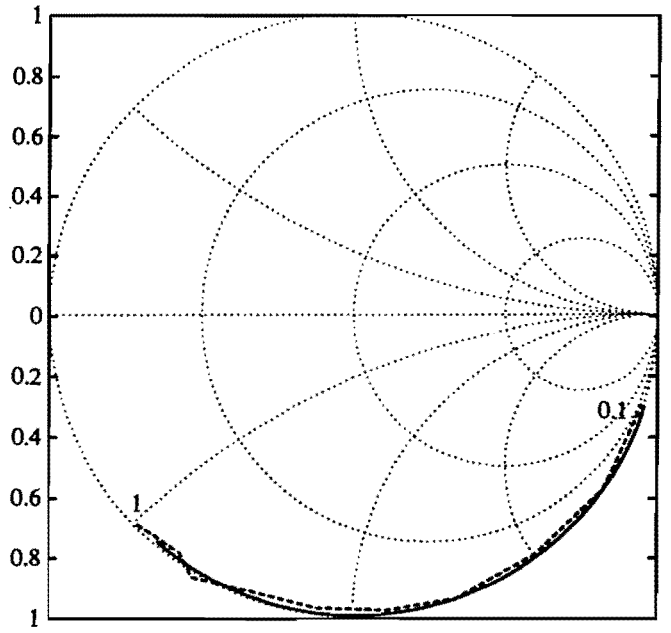


(a)

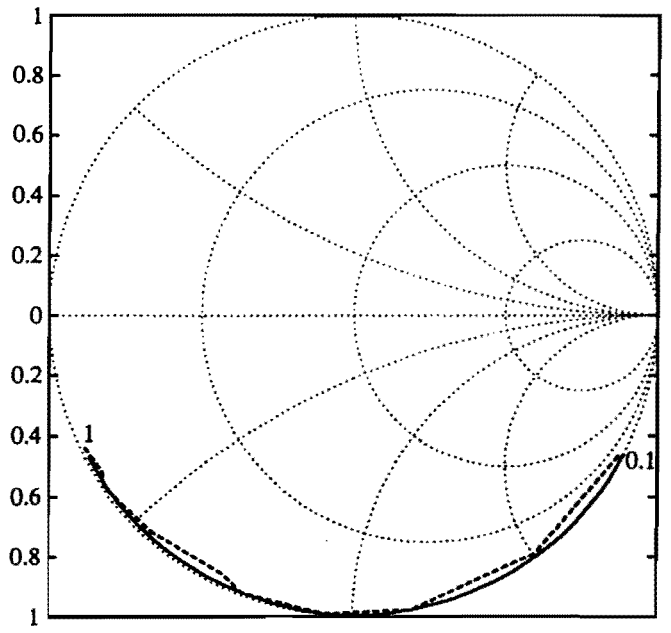


(b)

Figure 6.5 FDR measurement results for (a) C_1: 1 pF (b) C_2: 2.2 pF.

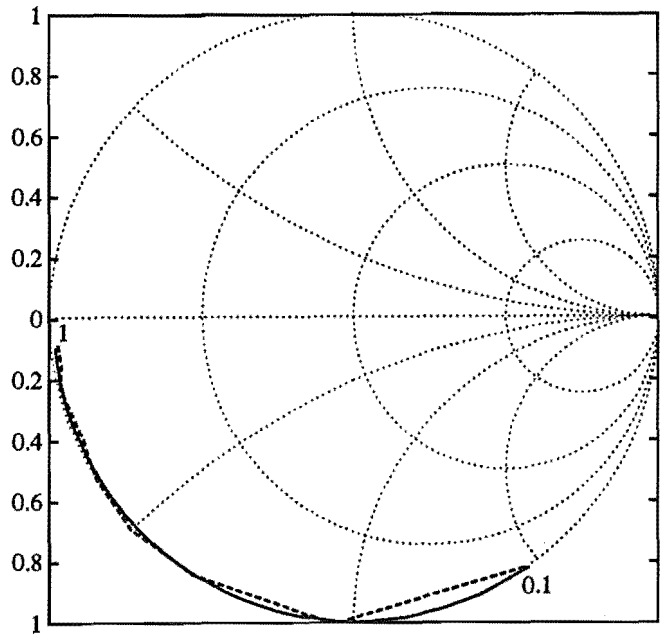


(a)

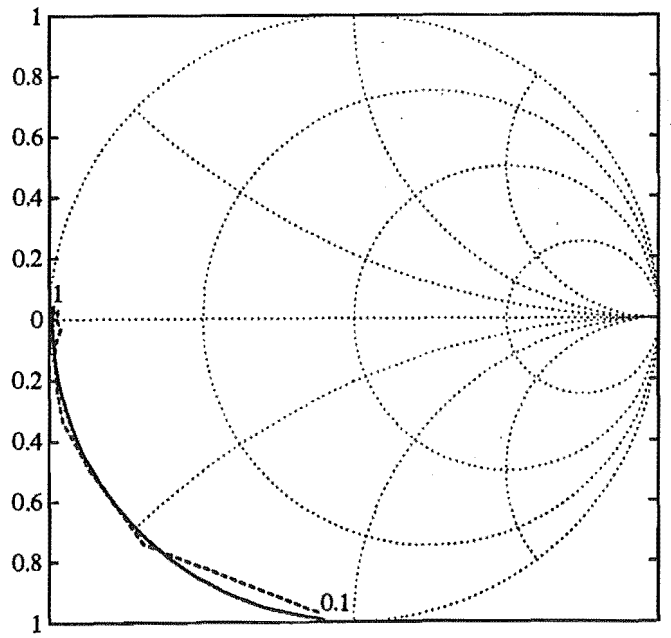


(b)

Figure 6.6 FDR measurement results for (a) C_3: 4.7pF (b) C_4: 8.2pF.

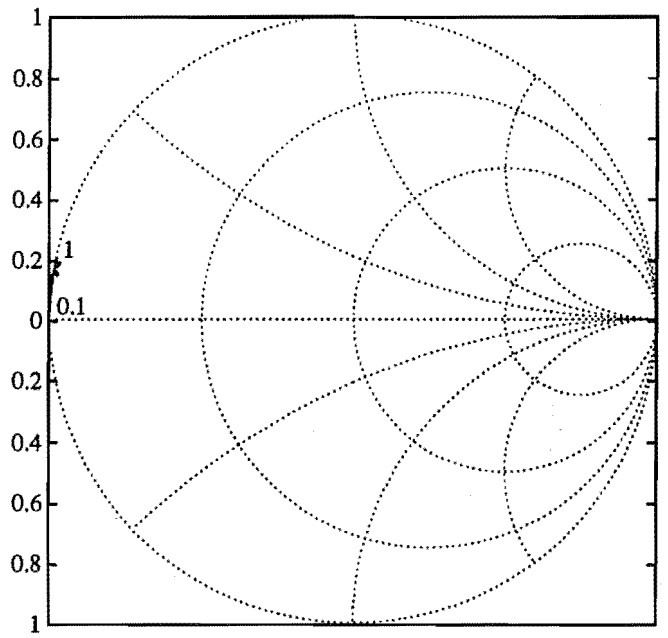


(a)

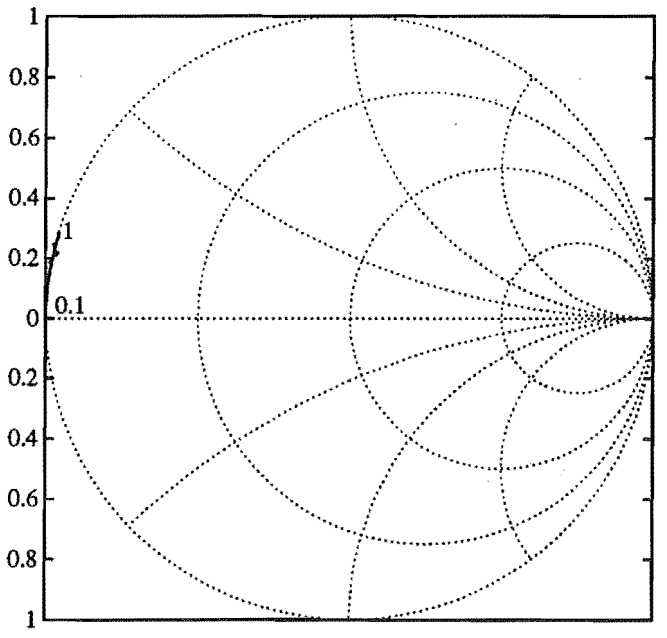


(b)

Figure 6.7 FDR measurement results for (a) C_5: 18 pF (b) C_6: 33 pF.

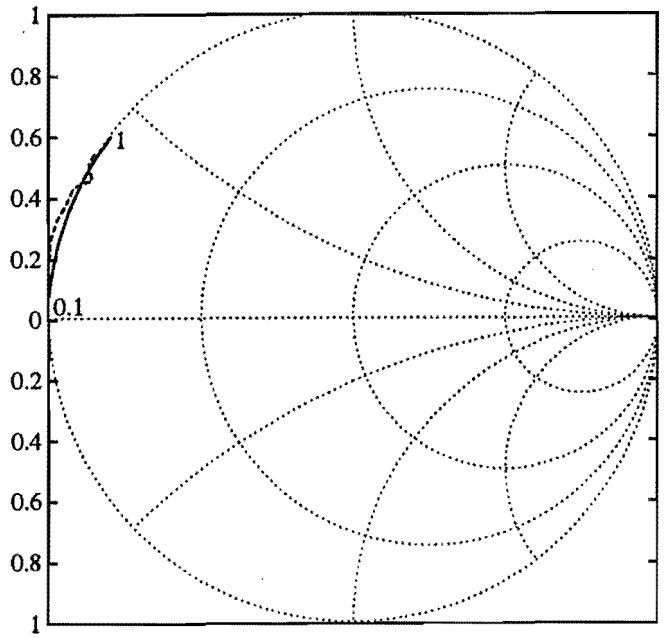


(a)

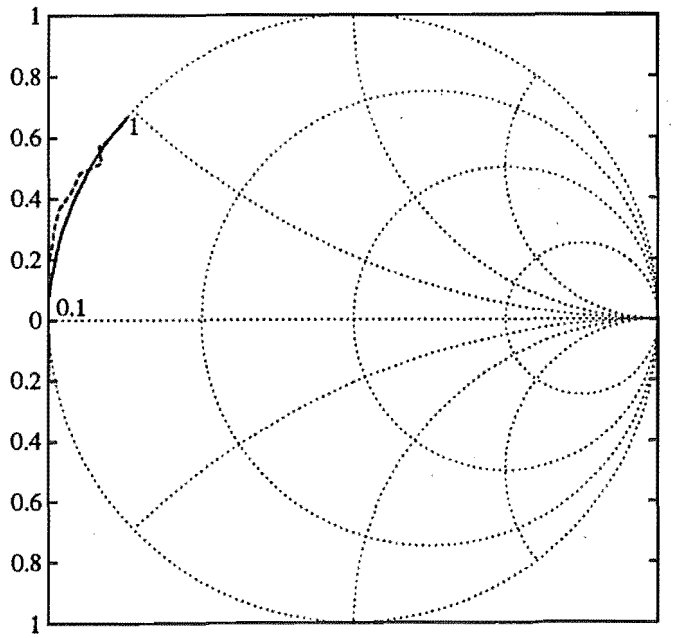


(b)

Figure 6.8 FDR measurement results for (a) L_1: 0.68nH (b) L_2: 1.92nH.

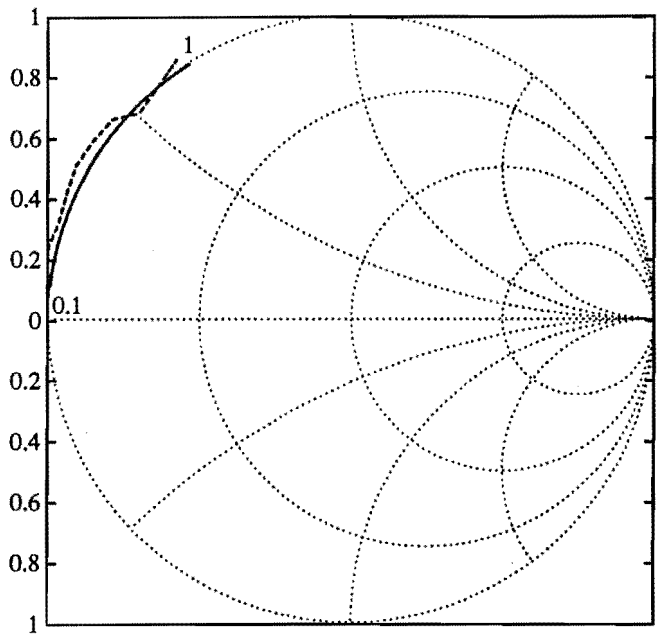


(a)

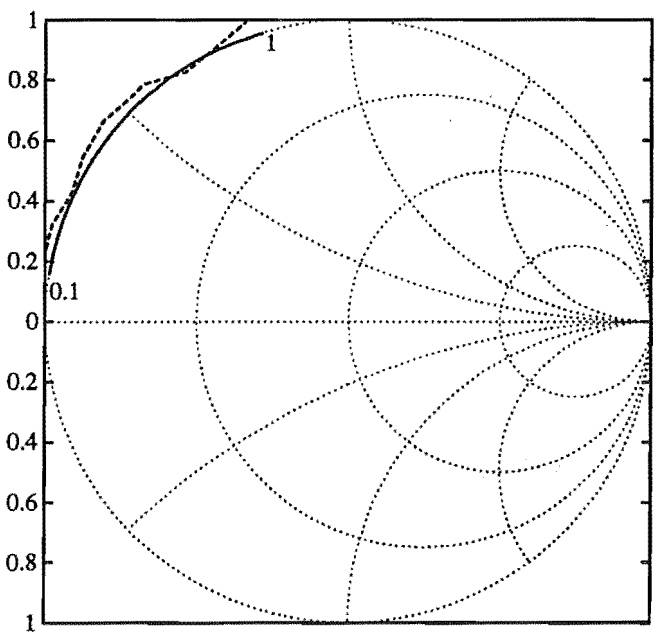


(b)

Figure 6.9 FDR measurement results for (a) L_3: 3.37 nH (b) L_4: 4.95 nH.

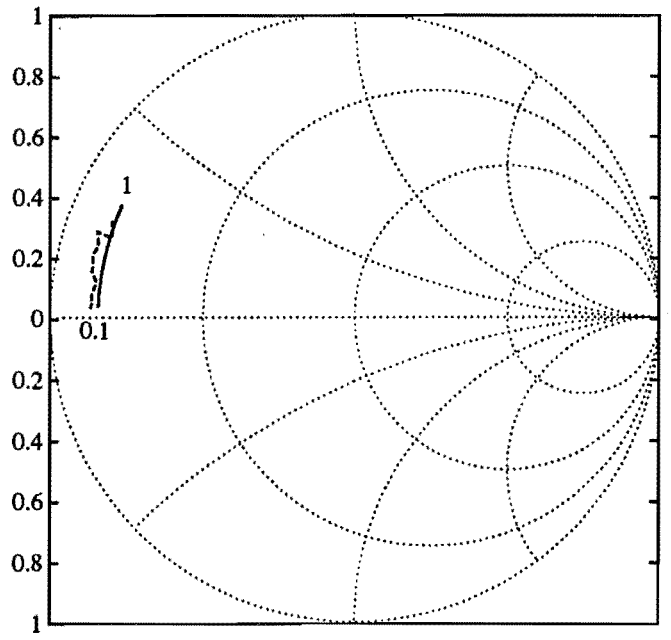


(a)

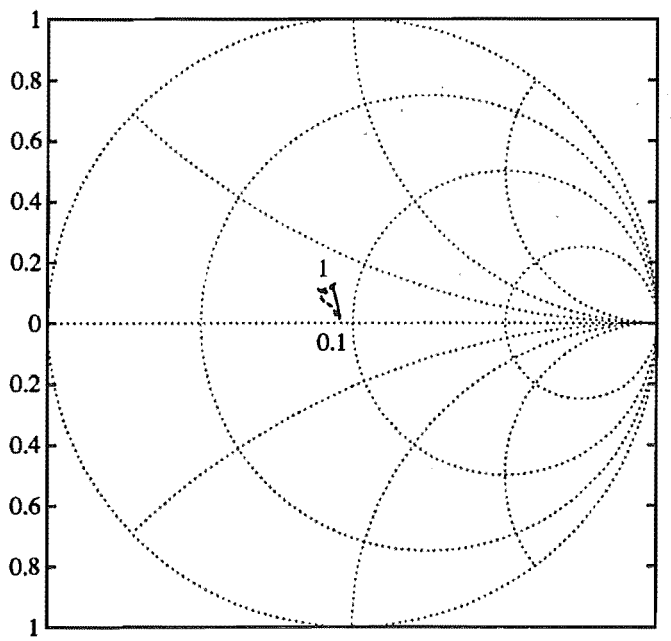


(b)

Figure 6.10 FDR measurement results for (a) L_5: 6.63 nH (b) L_6: 8.4 nH.

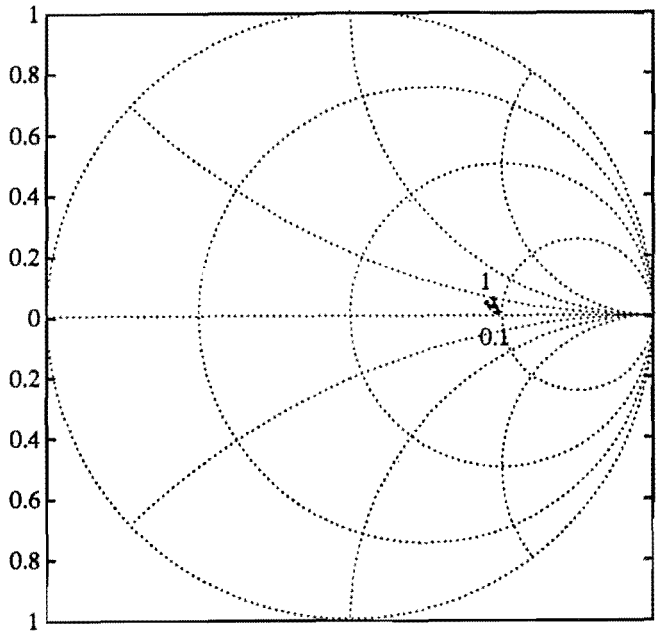


(a)

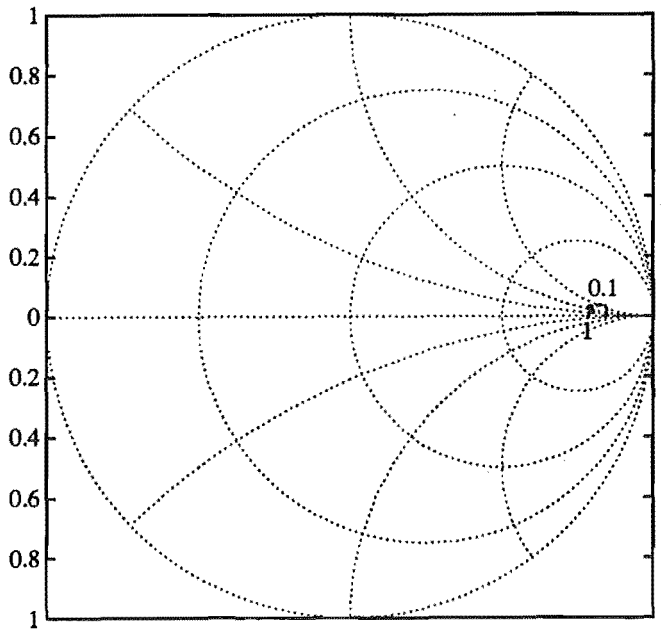


(b)

Figure 6.11 FDR measurement results for (a) R_1: 4.4 Ω (b) R_2: 46 Ω.

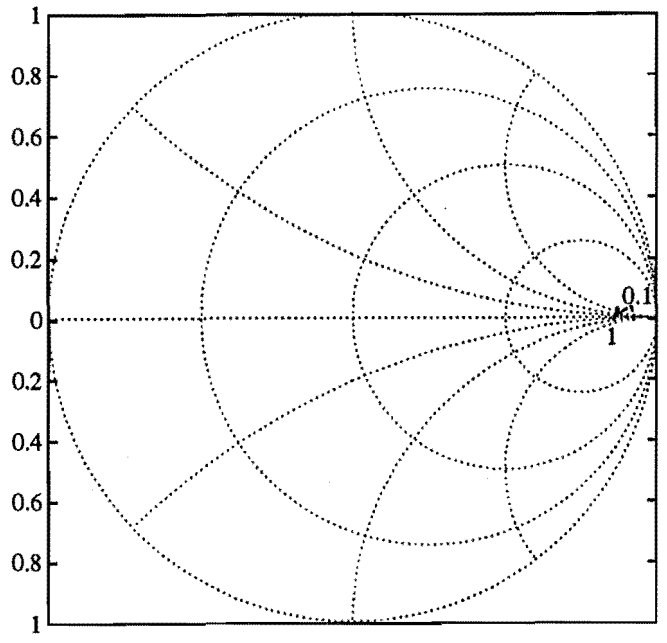


(a)

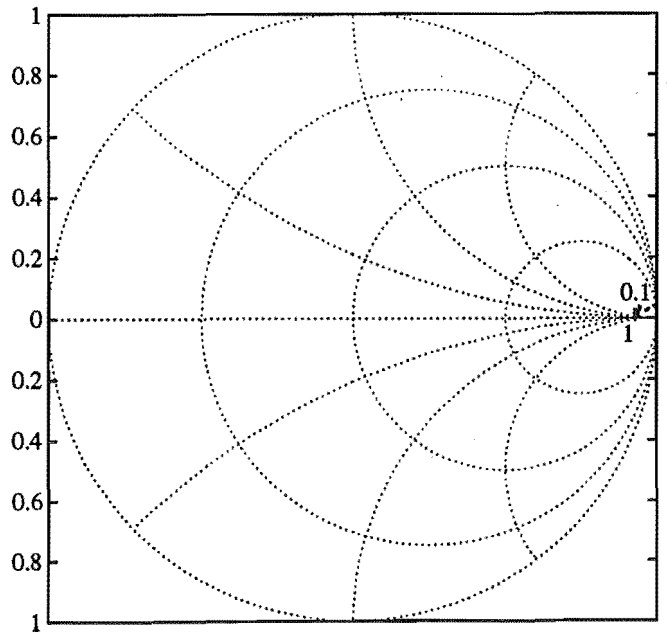


(b)

Figure 6.12 FDR measurement results for (a) R_3: 146 Ω (b) R_4: 444 Ω.



(a)



(b)

Figure 6.13 FDR measurement results for (a) R_5: 702 Ω (b) R_6: 1.49 kΩ.

± 0.5 degree, at a level of 50 dB below the reference. We believe this to be the least contribution to experimental error. The ANA at Auckland University is regularly calibrated using traceable standards, and is in regular use by experienced technicians. For this reason the ANA results are used as reference in this experiment.

3. Simplification of the SFG
   The SFG used in the computations was simplified from the complete SFG which includes all the S-parameters of each element in the configuration. The simplified SFG gives better results for the HP778D coupler than for the TFH prototypes because the HP778D coupler characteristic impedance is most closely matched to the normalizing impedance.

4. Inaccuracy of the vector voltmeter
   The HP8405A Vector Voltmeter has the following specification [HP APPLICATION NOTE 77–3, 1967]:

   - Uncertainty in magnitude ($|\Delta_{MV}(\Gamma_L)|$)

   $$|\Delta_{MV}(\Gamma_L)| \leq \pm(0.03 + 0.03|\Gamma_L|^2) \tag{6.6}$$

   for $0 < |\Gamma_L| < 1.0$.

   - Uncertainty in phase ($\Delta_{\phi V}(\Gamma_L)$)

   $$\Delta_{\phi V}(\Gamma_L) \leq \pm\left[2 + \sin^{-1}\frac{0.01}{|\Gamma_L|} + \sin^{-1}(0.03|\Gamma_L|^2)\right] \tag{6.7}$$

   for $0.01 < |\Gamma_L| < 1.0$.

   For example: for a pure reactive load $|\Gamma_L| = 1$, giving a magnitude uncertainty of ± 0.06 (or ± 0.5 dB), and phase uncertainty of ± 4.3 degrees.

   Equations 6.6 and 6.7 are reliable only when the Vector Voltmeter is regularly calibrated (typically every 12 months). The Vector Voltmeter at Canterbury University has not been calibrated since it was purchased in 1971. However, these equations are used to outline the Vector Voltmeter error bounds in the following discussion of measurement uncertainty. As will be seen later, even without calibration the results lie within these bounds except for the case of very small amplitude of Γ_L.

5. Connector reliability
   Because each BNC termination has been plugged and unplugged at least 600 to 1000 times, the characteristics are degraded to the detriment of measurement repeatability. No quantitative limits can be deduced without rigorous testing, but the author frequently observed uncertain connections and sensitivity of the

but the author frequently observed uncertain connections and sensitivity of the indicated readings to mechanical movement. Likely mechanisms are loss of surface plating leading to increased contact resistance in series with both the inner conductor and the outer coaxial elements, surface contamination by atmospheric pollution, and corrosion caused by human body salts deposited during handling.

6.4.2 The Measurement Uncertainty

The magnitude and phase deviations of the FDR measurement results are plotted in Figures 6.14 to 6.16, for 100, 500, and 900 MHz respectively. The magnitude deviations, $|\Delta_{MM}(\Gamma_L)|$ (%), are computed using equation 6.8, whereas the phase deviations, $\Delta_{\phi M}(\Gamma_L)$, are computed using equation 6.9.

$$|\Delta_{MM}(\Gamma_L)| = \frac{100\,(|\Gamma_L^{FDR}| - |\Gamma_L^{ANA}|)}{|\Gamma_L^{ANA}|} \tag{6.8}$$

$$\Delta_{\phi M}(\Gamma_L) = \phi_{\Gamma_L}^{FDR} - \phi_{\Gamma_L}^{ANA} \tag{6.9}$$

The deviations are plotted as bar charts; dashed lines being the specification bounds for the HP 8510 ANA; dash-dot lines the specification bounds of the HP8405A Vector Voltmeter, derived from equations 6.6 and 6.7. For comparison purposes, the magnitude error $|\Delta_{MV}(\Gamma_L)|$ has been converted into percentage by multiplying it by $\frac{100}{|\Gamma_L^{ANA}|}$.

From these plots, we can conclude that the technique described in this chapter is valid because the HP778D results are generally within the specification bounds of the measuring equipment. Deviations significantly increase when the magnitude of the reflection coefficient approaches zero. This can be clearly seen from the results for resistive loads, where maximum deviation occurs with $R_2 = 46\,\Omega$ ($|\Gamma_L| \leq 0.042$).

Deviations from the reference (ANA) results increase with frequency, indicating the effects of impedance mismatch. However, these are systematic errors that can be compensated for during calibration.

6.5 CONCLUSION

This chapter has described the FDR experiment with the prototype and commercial directional couplers. A Vector Voltmeter (HP8405A) has been used in this experiment. Measurement technique and detailed construction of the terminations and reference loads have been presented.

Reflections from impedance mismatches, together with the incomplete SFG of the measurement configuration, cause the prototype results to be outside the specification bounds of the measuring equipment. However, the HP778D results, which are comparable to the results obtained from the ANA, strengthen our confidence in the ultimate success of the technical improvements developed in this thesis.

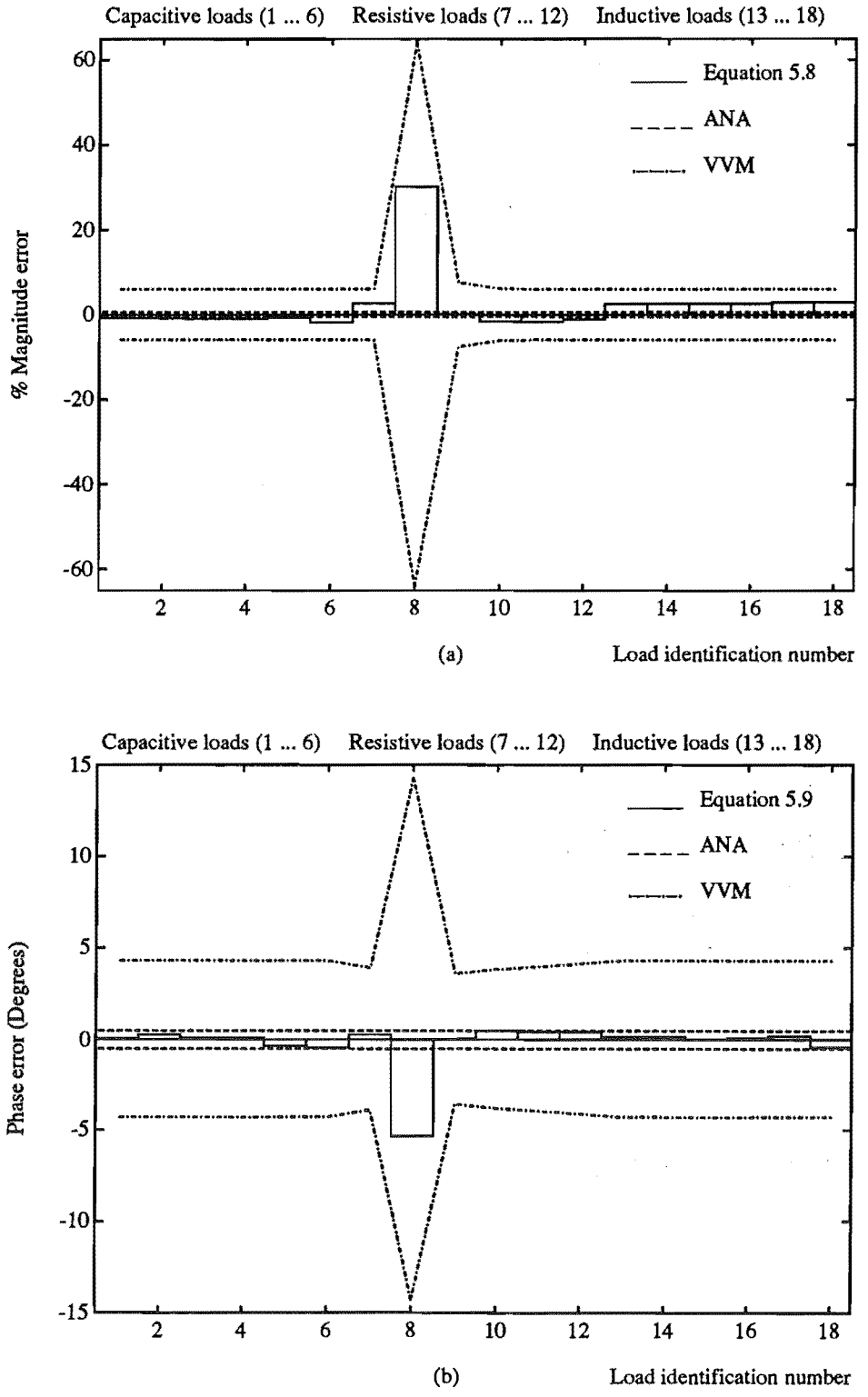


Figure 6.14 Deviations from ANA results at 100 MHz (a) magnitude (b) phase.

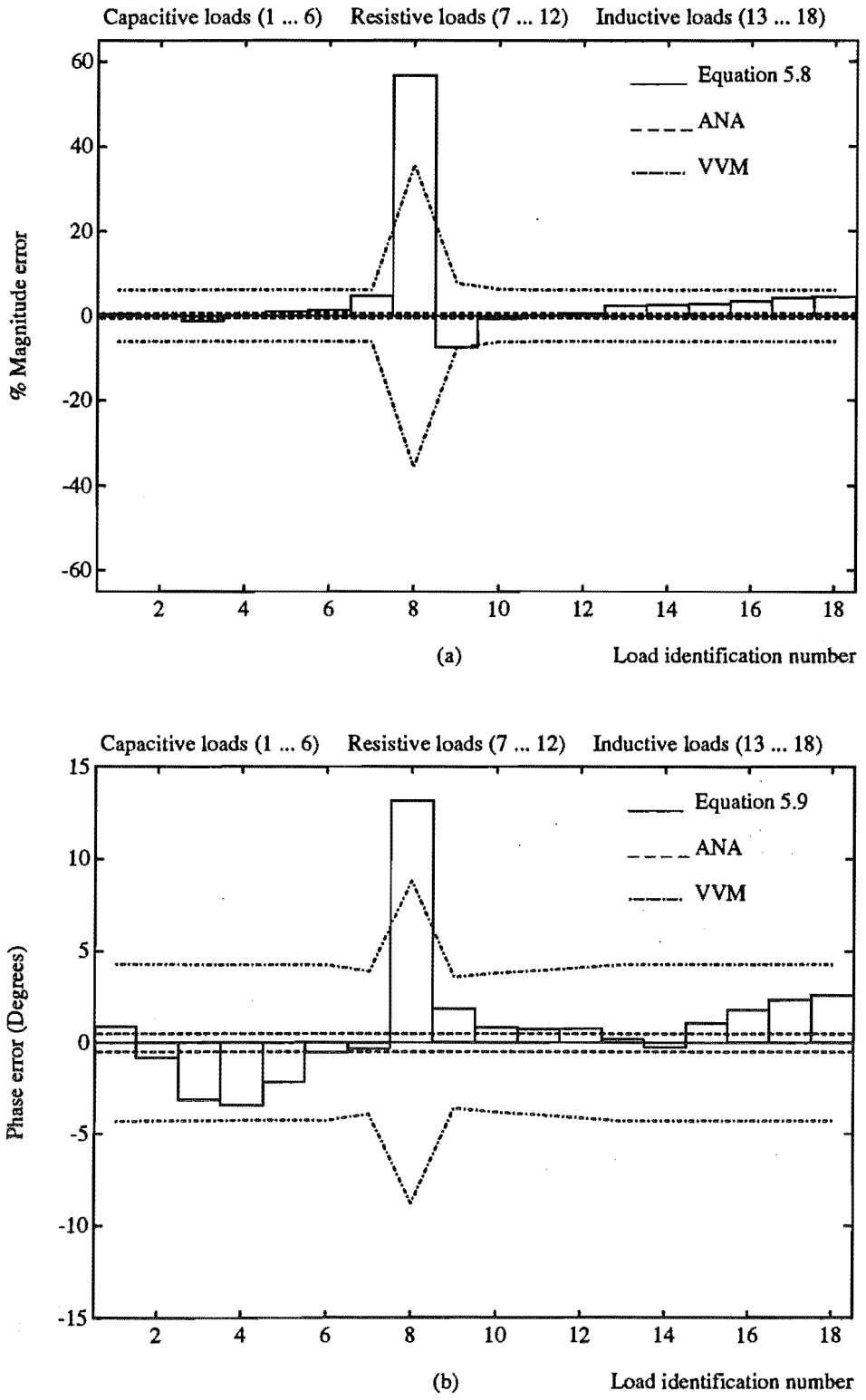


Figure 6.15 Deviations from ANA results at 500 MHz (a) magnitude (b) phase.

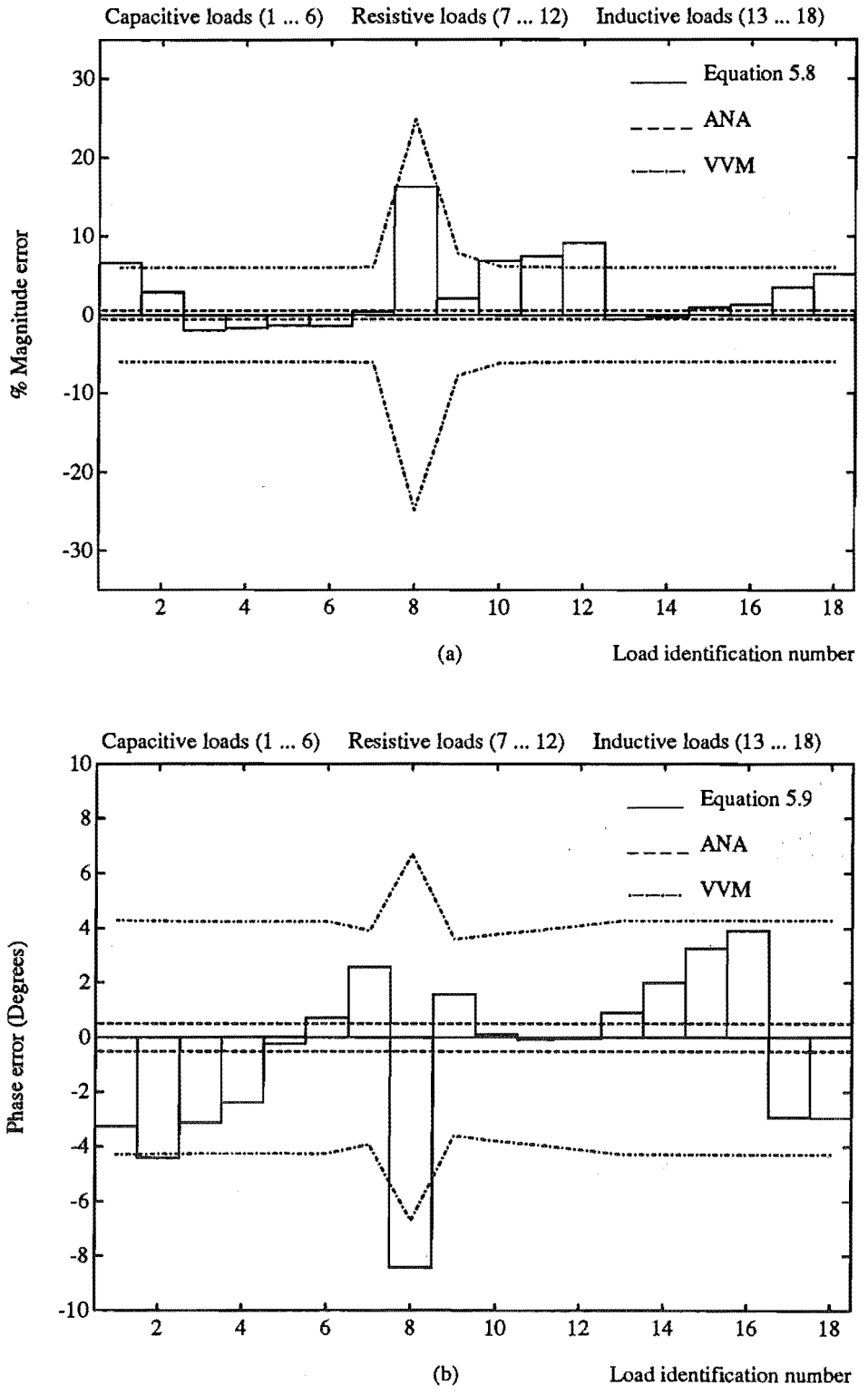


Figure 6.16 Deviations from ANA results at 900 MHz (a) magnitude (b) phase.

HP778D measurement results are compared with those obtained using the HP8510 Automatic Network Analyzer. The results demonstrate that a matched dual directional coupler can be used in such an application, yielding results comparable to those obtained using an automatic network analyzer.

Similar results can be expected from the prototype coupler when it has been fully optimized and more accurate test equipment becomes available.

CHAPTER 7

LOAD EQUIVALENT NETWORK MODELLING

The problem of determining the values of parameters which optimize (minimize or maximize)[1] some functions subject to various types of constraints is widespread. The study of these problems has reached a sophisticated level and an extensive literature exists, including a number of excellent text books.

The material presented in this thesis applies to optimization techniques used in circuit modelling. The main objective is to establish a strategy to obtain a circuit model which has frequency characteristics *close to* those measured using the method described in the previous chapter.

This chapter describes two optimization techniques, The pattern search of Hooke and Jeeves and the Nelder and Mead simplex algorithm, which may be used to obtain the value of each element in the selected load model. Section 7.1 introduces the basic processes used in network optimization. To aid the reader, some fundamental concepts, definitions, and symbols used in this thesis are given in section 7.2.

Section 7.3 reviews general iterative methods in network optimization. Then, the DUT load modelling technique using optimization methods is presented in section 7.4. The two chosen algorithms are demonstrated, based on an example load model. The results are presented and discussed in sections 7.5, 7.6 and 7.7.

The material in sections 7.1 to 7.3 has been collated from many sources so as to present a unified theory in readily accessible form. The author lays no claim to originality regarding this material or form of presentation. The reader who is already familiar with optimization theory may proceed directly to section 7.4 which describes the application of optimization techniques in DUT load modelling.

[1] An optimum point of a function can be either a maximum or a minimum point of that function.

7.1 INTRODUCTION TO COMPUTER-AIDED NETWORK OPTIMIZATION

In many practical network design or synthesis problems, the network function is not available analytically, but rather as a set of data obtained experimentally or from a simulation. Furthermore, analytical design or synthesis procedures do not take into account constraints imposed by element value, noise level, cost, sensitivity and the like. These drawbacks, together with the lack of a general analytical method for the design of time-varying and nonlinear networks, have necessitated new design techniques based on iterative methods. These techniques use a digital computer to carry out the design processes, namely Computer-Aided-Design (CAD).

Fully automated design and optimization is certainly an ultimate goal of CAD. The main advantage of computer-aided network optimization techniques over traditional network design, is their flexibility. They can incorporate various constraints imposed on the final network, can lead to compromise solutions, can (in most cases) reconcile conflicting requirements carrying different weights, and can accommodate prescribed active elements, nonlinearities, and parasitics [BANDLER, 1969].

Typically, a desired network topology is chosen and tentative values are assigned to the elements. Then, in each iteration, these values are altered in such a way that a preassigned error function is reduced. This iterative process is continued until the error function is minimized. A major disadvantage of computer-aided optimization is that generally there is no guarantee that the iterations will converge to an optimal network.

Figure 7.1 illustrates the basic optimization process, which has been applied to network modelling as described in the following sections.

7.2 FUNDAMENTAL CONCEPTS AND DEFINITIONS IN OPTIMIZATION PROBLEMS

This section provides a brief overview of concepts, some of the fundamental considerations and general mathematical definitions used in optimization problems.

7.2.1 Terminology

The procedures to be discussed are concerned with minimization of a single function $\boldsymbol{E}$. Minimizing a function is the same as maximizing the negative of the function, so there is no loss in generality. In general, $\boldsymbol{E}$ is called the objective function, or cost function, which in some way embodies a set of design criteria. In particular, $\boldsymbol{E}$ will be a measure of the error or difference between the desired response $\boldsymbol{F}$ and the response $\widehat{\boldsymbol{F}}^i$ at i^{th} iteration. $\widehat{\boldsymbol{F}}^i$ is usually a function of two sets of variable [TEMES and CALAHAN, 1967]:

1. The parameters p_i; $i = 1, 2, \ldots, n$, are denoted by the vector

$$\boldsymbol{p} \triangleq [p_1,\ p_2,\ \cdots,\ p_n]^T \tag{7.1}$$

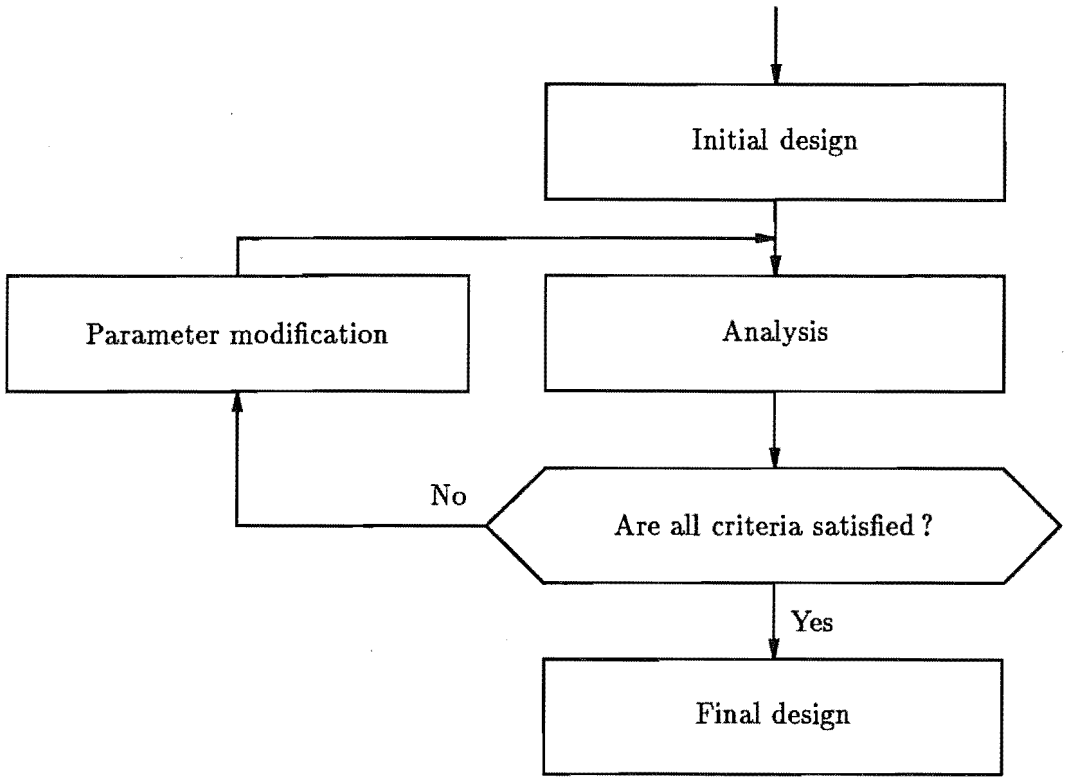


Figure 7.1 Flow chart of an optimization process.

where n is the number of parameters which are to be adjusted to minimize $\boldsymbol{E}$.

2. The independent variables x_i; $i = 1, 2, \ldots, m$, are denoted by

$$\boldsymbol{x} \triangleq [x_1,\ x_2,\ \ldots,\ x_m]^T \tag{7.2}$$

where m is the number of sample points. The vector $\boldsymbol{x}$ may, for example, represent a set of frequencies, times, or positions where $\boldsymbol{F}$ and $\hat{\boldsymbol{F}}^i$ are measured or calculated.

In most scientific and engineering problems, physical measurements of the objective function $\boldsymbol{E}$ are taken as a series of values as the independent variable $\boldsymbol{x}$ is varied. The number of samples m may be limited, due either to practical difficulties in making measurements, or disturbance of the system by the measurement process. In most cases, the number of measurement points m is kept to be minimum or just sufficient to satisfy the requirements.

$\boldsymbol{E}$ will in general be written $\boldsymbol{E}(\boldsymbol{p}, \boldsymbol{x})$, or simply $\boldsymbol{E}(\boldsymbol{p})$ when the independent variable designation is unimportant.

Some optimization methods require gradient information about the objective function $\boldsymbol{E}$. This is obtained in the form of first and second order partial derivatives of $\boldsymbol{E}$ with respect to the n parameters. The gradient vector $\nabla \boldsymbol{E}$ which is a column vector

of first order partial derivatives, is denoted by G where

$$G(\boldsymbol{p}, \boldsymbol{x}) \triangleq \left[\frac{\partial E}{\partial p_1}, \frac{\partial E}{\partial p_2}, \ldots, \frac{\partial E}{\partial p_n}\right]^T \tag{7.3}$$

The $n \times n$ symmetric matrix of second order partial derivatives of E is known as the *Hessian matrix* and is denoted by

$$H \triangleq \begin{bmatrix} \frac{\partial^2 E}{\partial p_1{}^2} & \frac{\partial^2 E}{\partial p_1 \partial p_2} & \cdots & \frac{\partial^2 E}{\partial p_1 \partial p_n} \\ \frac{\partial^2 E}{\partial p_2 \partial p_1} & \ddots & & \vdots \\ \vdots & & \ddots & \vdots \\ \frac{\partial^2 E}{\partial p_n \partial p_1} & \cdots & \cdots & \frac{\partial^2 E}{\partial p_n{}^2} \end{bmatrix} \tag{7.4}$$

During the optimization process, the *search direction* and the *step-size parameter* must be determined. They are defined here as

$$\boldsymbol{d} \triangleq [d_1, d_2, \ldots, d_n]^T \tag{7.5}$$

and

$$\boldsymbol{s} \triangleq [s_1, s_2, \ldots, s_n]^T \tag{7.6}$$

respectively. The step-size parameter can be either scalar where every parameter has the same step size, or vector where each parameter has a different step size.

7.2.2 Geometry

In general, there will be *constraints* that must be satisfied either during optimization or by the final solution. A *hard constraint* is one that must not be violated either at the final answer or during the optimization process. A *soft constraint* is one that may be violated either during the searching process or possibly at the final answer [BRAYTON and SPENCE, 1980].

Each parameter may be constrained explicitly by upper and lower boundaries as follows:

$$p_{li} \leq p_i \leq p_{ui} \tag{7.7}$$

where $i = 1, 2, \ldots, n$, p_{li} and p_{ui} are lower and upper bounds respectively. Furthermore, the problem could be constrained by a set of c implicit functions ($c < n$)

$$c(\boldsymbol{p}) \geq 0 \tag{7.8}$$

A vector $\boldsymbol{p}$ which satisfies the constraints is termed a *feasible vector.* It lies in a *feasible region* $\mathcal{R}$ (closed if equalities are included as in equation 7.7 or 7.8, otherwise open). A region in which the constraints are not satisfied is termed a *non-feasible* or *infeasible region.* It is assumed that $E(\boldsymbol{p})$ can be obtained either by calculation or by measurement.

A geometrical representation of an error function may be used as a conceptual aid to visualize optimization procedures. The two most widely used representations are the *error* or *cost surface* corresponding to the multivariable function $E(p)$, and the *contour lines* of the same function for various fixed values of E. These can be easily illustrated for $n = 1$ or $n = 2$. Figure 7.2 shows a contour representation illustrating some features encountered in optimization problems. The feasible region, which is bounded by both linear and nonlinear constraints, contains one global minimum, one local minimum and one saddle point (in this example $E_1 > E_2 > E_3$ and so on). In higher dimensions, such geometrical aids have little practical value.

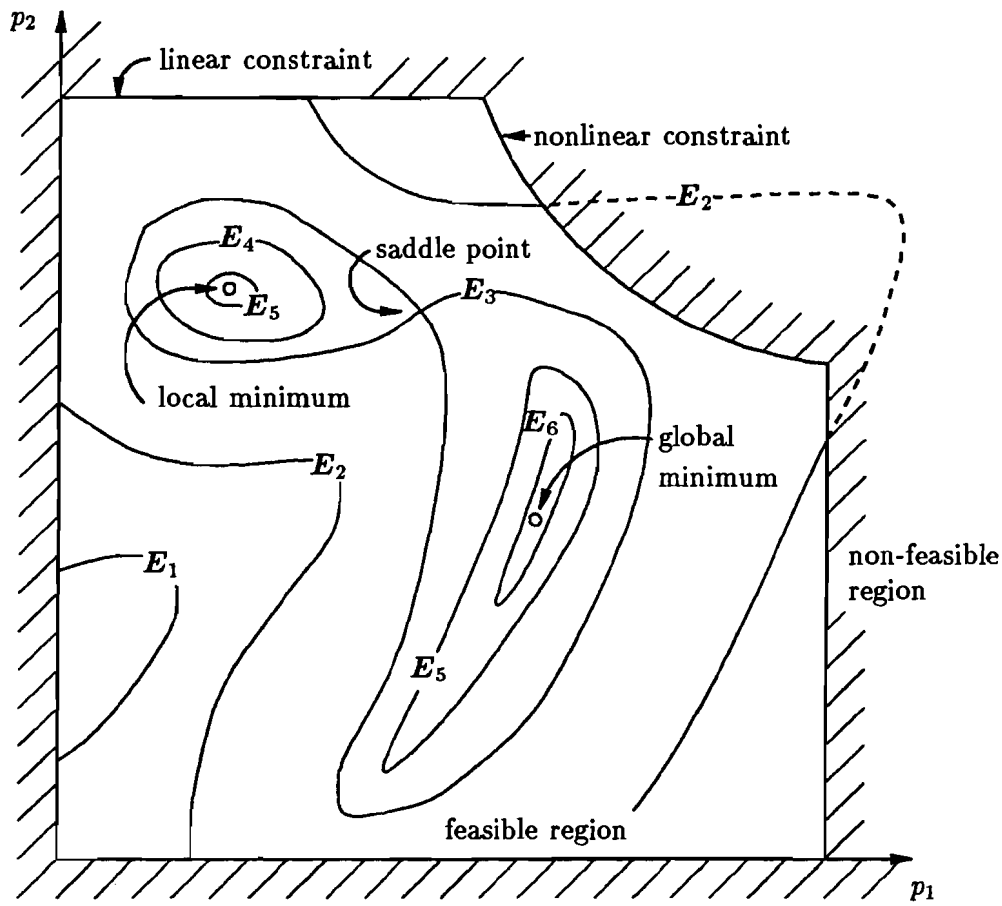


Figure 7.2 Contour representation of a two-dimensional ($n = 2$) objective function.

7.2.3 Convexity and Unimodality

A *unimodal* function may be defined as one which has a unique optimum in the feasible region. Its unimodality is not affected by the presence of discontinuities in the function or its derivatives. A function which has two optimum points is termed *bimodal* and one which has more than two optima in the feasible region is termed *multimodal* function.

Figure 7.3 shows typical unimodal functions of one variable.

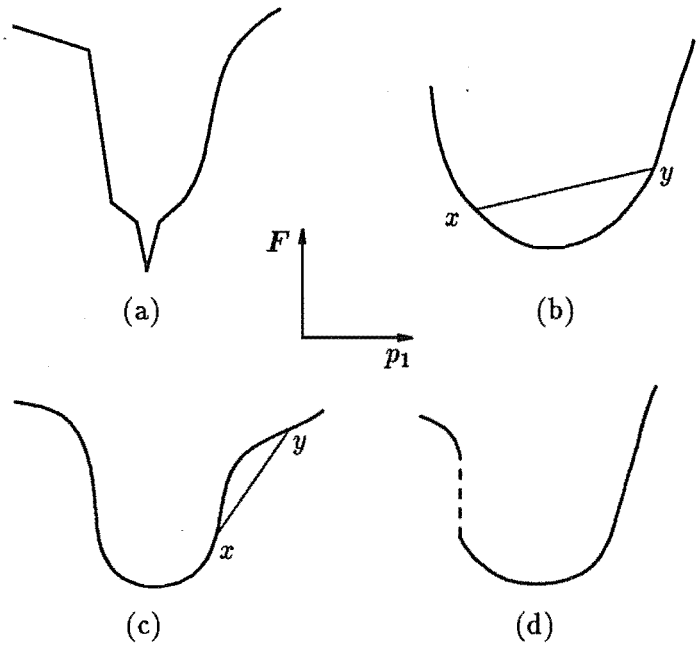


Figure 7.3 Typical unimodal functions (a) a unimodal function (b) a continuous convex function (c) a continuous non-convex function (d) a discontinuous function.

Figure 7.3 (b) shows a continuous *convex* function with continuous derivatives. In geometrical terms a function is *strictly convex* if the straight line connecting any two points on that graph, for example the line between points x and y in Figure 7.3 (b), lies above the graph. In mathematical terms, a single variable function is convex if for all x and y and all values λ $(0 < \lambda < 1)$,

$$\boldsymbol{F}(\lambda x + (1-\lambda)\, y) \;\leq\; \lambda \boldsymbol{F}(x) + (1-\lambda)\boldsymbol{F}(y) \tag{7.9}$$

If the equality is not included, $\boldsymbol{F}$ is termed *strictly convex*. The function is concave if $-\boldsymbol{F}$ is convex [ADBY and DEMPSTER, 1974]. If the first derivatives of the function exist then strict convexity implies that the Hessian matrix is positive-definite[2] and vice versa [BANDLER, 1969].

7.2.4 Constraints

A discussion on how to deal with constraints in optimization is appropriate here, because the constraint characteristics and the way they associate with the problem can be a deciding factor in the selection of an optimization strategy. In practice, one seldom finds unconstrained problems.

[2]When a matrix A is positive-definite (positive-semidefinite), $A > 0$ $(A \geq 0)$.

There is no intention to discuss all the techniques for constrained optimization, since this topic is a large and growing one. Emphasis will be placed on the particular methods of reducing a constrained problem into an essentially unconstrained one. The constraints are limited to linear explicit constraints in the form of lower and upper boundaries for each parameter such as that defined in equation 7.7, since they are probably the most frequently occurring constraints in circuit design problems. Other forms of constraint are discussed adequately in texts, such as [ADBY and DEMPSTER, 1974; SORENSON and KOBLE, 1976; BRAYTON and SPENCE, 1980].

A technique commonly used for such simple constraints is to introduce new variables so that the constrained problem transforms into an unconstrained one in the new variables, without altering the objective function.

We may define $\acute{p}_i$ such that [BOX, 1966]

$$p_i = p_{li} + (p_{ui} - p_{li}) \sin^2 \acute{p}_i \tag{7.10}$$

where $-\infty < \acute{p}_i < \infty$ but where only solutions within the range $[p_{li}, p_{ui}]$ are allowed. If the periodicity caused by this transformation is undesirable, one can try

$$p_i = p_{li} + \frac{1}{\pi}(p_{ui} - p_{li}) \cot^{-1} \acute{p}_i \tag{7.11}$$

This nonlinear transformation has a penalizing effect on the parameters near the upper and lower bounds. So if the optimum values are expected to lie away from the boundaries, this transformation may introduce a favourable parameter scaling [BANDLER, 1969].

When the constraints are in the form

$$p_i \geq p_{li} \tag{7.12}$$

one can use

$$p_i = p_{li} + \acute{p}_i^2 \tag{7.13}$$

For

$$p_i \geq 0 \tag{7.14}$$

one can employ a simple relation such as

$$p_i = p_{li} + e^{\acute{p}_i} \tag{7.15}$$

Other forms of variable transformation can be found, such as those described in [BOX, 1966; BRAYTON and SPENCE, 1980]. These techniques should be used when one expects the minimum to be far away from the constraints, because such nonlinear transformations will make optimization problems harder to solve when a minimum lies near or on some constraint.

7.2.5 Error Criteria and Weights

The objective function is formulated from the measured or calculated values of all sample points. There are several methods of objective function formulation. Only one of these methods, the least $\mathcal{P}^{th}$ method, frequently used in network design, will be presented. Other methods, such as minimax or formulation in terms of inequality constraints, are described by BANDLER [1969].

7.2.5.1 Weighting factors

A discussion of weighting factors is appropriate at this stage. Essentially, their purpose is to emphasize or deemphasize various parts of the response to suit the designer's requirements. They are also used in the case of several independent variables to equalize the effects of error when the corresponding function values give errors on a greatly different scale as different independent variables change.

7.2.5.2 Least $\mathcal{P}^{th}$ approximation

A frequently employed class of objective functions may be written in the generalized form [BANDLER, 1969]

$$\begin{aligned} E(\boldsymbol{p},\boldsymbol{x}) &= \sum_{i=1}^{m} \left| W_i(\boldsymbol{x}) \left(\widehat{F}_i(\boldsymbol{p},\boldsymbol{x}) - F_i(\boldsymbol{x}) \right) \right|^{\mathcal{P}} \\ &= \sum_{i=1}^{m} |e_i(\boldsymbol{p},\boldsymbol{x})|^{\mathcal{P}} \end{aligned} \tag{7.16}$$

The subscript i refers to quantities evaluated at the sample points $\boldsymbol{x}_i; i = 1, 2, \ldots, m$. Thus the objective is to minimize the sum of the magnitudes enlarged by some power $\mathcal{P}$ of the weighted deviations $e_i(\boldsymbol{p})$ of the network response from a desired response over a set of sample points $\boldsymbol{x}_i$. $\mathcal{P}$ may be any positive integer.

Sample points are commonly spaced uniformly along the $\boldsymbol{x}$ axis in the interval $[\boldsymbol{x}_l, \boldsymbol{x}_u]$. If the objective is to minimize the area under a curve then sufficient sample points must be used to ensure that equation 7.16 is a good approximation to the area. However, one should remember that function evaluations are often the most time consuming parts of an optimization process. Therefore, the number of sample points should be carefully chosen for the particular problem under consideration. This consideration applies to any objective function formulation which involves sampling.

With $\mathcal{P} = 1$ equation 7.16 represents the area under the deviation magnitude curve if sufficient sample points are used. With $\mathcal{P} = 2$ we have a *least squares* type of formulation. The higher the value of $\mathcal{P}$ the more emphasis will be given to those deviations which are largest. If the requirement is to concentrate more on minimizing the maximum deviation, a sufficiently large value of $\mathcal{P}$ must be chosen. In practice, a value of $\mathcal{P}$ from 4 to 10 may provide an adequate approximation for engineering purposes to the ideal objective [BANDLER, 1969]. A good choice of the weighting factors W_i will

also assist in emphasizing or deemphasizing parts of the response deviation. Changing the objective function formulation, number of sample points, or weighting factors may result in a more satisfactory optimum.

7.2.6 Terminating Criteria

A search must be terminated according to some prescribed criterion. Since the minimum value of the objective function is usually not known beforehand, a number of different termination criteria can be defined. Some are an inherent part of the search procedure itself. More often termination occurs as a result of the satisfaction of one or more of the following criteria [SORENSON, 1976].

7.2.6.1 Change in objective function

The search can be terminated when the change in the value of the objective function for successive steps becomes less than a prescribed tolerance.

$$E(\boldsymbol{p}_i) - E(\boldsymbol{p}_{i+1}) \quad < \quad \epsilon_{obj} \tag{7.17}$$

where $\epsilon_{obj} > 0$. If the objective function changes very slowly in the vicinity of the minimum, this criterion can result in termination although the trial point $\boldsymbol{p}_{i+1}$ is a substantial distance from the minimizing point $\boldsymbol{p}_{\min}$.

7.2.6.2 Value of gradient

A necessary condition for a minimum is that the gradient vanishes at $\boldsymbol{p}_{\min}$. It is therefore reasonable to terminate the search when the magnitude of the gradient is less than a prescribed tolerance.

$$\left\| \frac{\partial E}{\partial \boldsymbol{p}}(\boldsymbol{p}_{\min}) \right\| \quad \leq \quad \epsilon_{grad} \tag{7.18}$$

where $\| \star \|$ denotes magnitude of $\star$ and $\epsilon_{grad} > 0$. This criterion is not appropriate for direct search methods since the gradient is not computed. Also, if the objective surface is flat in the vicinity of the minimum $\boldsymbol{p}_{\min}$, the termination may be a very sensitive function of the threshold parameter ϵ_{grad}.

7.2.6.3 Change in trial point

The step-size parameter can provide an indication of the distance from the minimum. Then, the search may be terminated when the step size becomes less than some assigned tolerance.

$$\|\boldsymbol{p}_{i+1} - \boldsymbol{p}_i\| \quad < \quad \epsilon_{step} \tag{7.19}$$

where $\epsilon_{step} > 0$. Note that the distance $\|\boldsymbol{p}_{i+1} - \boldsymbol{p}_i\| = \|\boldsymbol{s}_i\| \, \|\boldsymbol{d}_i\| = \|\boldsymbol{s}_i\|$ when $\|\boldsymbol{d}_i\| = 1$. When the search direction is normalized, the magnitude of the step-size parameter can be used to establish termination of the search.

The conditions from equation 7.17- 7.19 can be implemented in a variety of ways to establish a specific termination criterion.

7.2.7 Convergence

To compare different optimization techniques, one should consider the following questions [ADBY and DEMPSTER, 1974].

1. Has the value $\boldsymbol{E}$ of the objective function converged to a minimum and is this minimum a global minimum ?
2. What was the speed of convergence ?

The value of $\boldsymbol{E}$ for successive iterations will in most cases be the only available guide to the progress of the optimization. When $\boldsymbol{E}$ does not reduce over a number of iterations, progress has clearly stopped and some kind of minimum has been reached. It is almost impossible to predict if the minimum reached is the global minimum. None of the optimization techniques will guarantee convergence to the global minimum especially for multimodal functions. Extensive testing of all minima found is not a complete solution, because the chosen algorithm may never converge to the global minimum of that particular function.

The relative speed of convergence is usually assessed by the number of evaluations of the error function $\boldsymbol{E}$, since the time required for a given computer to reach a solution is largely dominated by function evaluations. For gradient mehods, one must consider both the function and its partial derivatives evaluations.

7.3 ITERATIVE METHODS IN COMPUTER-AIDED DESIGN

This section discusses general iterative methods used in almost all computer-aided design techniques. To introduce the basic idea underlying these methods, let us consider a design of linear time-invariant networks operated under steady-state sinusoidal excitation.

The problem of determining the parameter vector $\boldsymbol{p}$ such that the error function $\boldsymbol{E}$ is minimized, is nontrivial especially for multivariable functions. The search methods generate trial points recursively. In particular, if a trial point $\boldsymbol{p}_i$ is known, a new trial point $\boldsymbol{p}_{i+1}$ is generated according to

$$\boldsymbol{p}_{i+1} = \boldsymbol{p}_i \pm \boldsymbol{s}_i \boldsymbol{d}_i \tag{7.20}$$

where $\boldsymbol{d}_i$ defines the *search direction* and $\boldsymbol{s}_i$ is the *step-size parameter*. The multiplication $\boldsymbol{s}_i \boldsymbol{d}_i$ is element-by-element product of the two vectors. The complete definition of a search procedure based on equation 7.20 involves four basic considerations:

- Choosing an initial trial point

- Determination of the search direction
- Selection of the step-size parameter
- Specification of the criteria for terminating the search

The following steps are involved in a typical iteration process.

1. Make a reasonable guess at the element values; that is, choose some initial values for R_i, C_i, and L_i. With this choice, the analysis techniques can be used to compute $\hat{\boldsymbol{F}}(\boldsymbol{p}_i, j\omega)$ which in turn will lead to the value of the objective function $\boldsymbol{E}$.

   No general rules exist for accomplishing this selection. The selection of $\boldsymbol{p}_1$ generally is guided by one's understanding of the problem itself. This initial guess need not be close to the optimal values. However, if, through experience or practical considerations, the user is able to make a reasonable guess, the number of iterations (and hence computation time) will be reduced. In many cases it is highly desirable to begin a search from a number of different initial trial points. Then, the outcome of each search can be compared and one can attempt to evaluate the influence of the initial point and to establish the minimizing solution. It is important to realize that the performance of an algorithm can be strongly influenced by the choice of $\boldsymbol{p}_1$.

2. Testing for convergence, using the value of the objective function $\boldsymbol{E}(\boldsymbol{p}_i)$ computed in step 1 and the prescribed criteria for terminating the search. If $\boldsymbol{E}(\boldsymbol{p}_i)$ satisfies all the prescribed criteria, the problem is solved; the element values chosen in step 1 are satisfactory. This situation, however, is unlikely to happen for a relatively complicated network. In this case we must proceed to step 3.

3. The search direction $\boldsymbol{d}_i$ and step-size parameter s_i are next defined using methods such as those described in section 7.6. A new trial point $\boldsymbol{p}_{i+1}$ is then determined from the previous trial point, the direction, and the step-size parameter.

4. Use the new element values, $\boldsymbol{p}_{i+1}$, to compute the objective function $\boldsymbol{E}(\boldsymbol{p}_{i+1})$. Test for termination using the same condition as in step 1, if the condition is satisfied stop the iterations; $\boldsymbol{p}_{i+1}$ is the optimal parameter vector. If not, the search must continue until convergence occurs or a set maximum iteration count exceeded.

7.4 LOAD MODELLING USING OPTIMIZATION TECHNIQUES

This section describes how a load model can be obtained using an optimization technique. Although the technique described here can be used with arbitrary load models, including nonlinear loads, the measured reflection coefficients will indicate only a linear

approximation to that load near the *d.c.* level of the small signal used in the measurement. Therefore, the following discussion assumes that a linear approximation can be made.

7.4.1 Problem Definition

We consider a network whose transfer function $\hat{\boldsymbol{F}}(\boldsymbol{p}, \jmath\omega)$ is to approximate a prescribed transfer function $\boldsymbol{F}(\boldsymbol{p}, \jmath\omega)$ over the frequency range of interest $[\omega_l, \omega_u]$. In this case, frequency is an independent variable which is the same as $\boldsymbol{x}$ defined in section 7.2.1.

Suppose that the topology and element types of the desired network are specified, in this case as in Figure 7.4. The parameters $\boldsymbol{p}$ defined in section 7.2.1 are the elements in the topology of the desired network.

From a design point of view this information may be collected by considering various constraints, such as cost, size, reliability, sensitivity, and availability of the elements. A design engineer can generally choose a reasonable topology and element type for the desired network. In our particular application and from a testing point of view, similar considerations can be applied by a test engineer. He can choose a reasonable topology and element type for his DUT input model. Furthermore, he can add constraints such as upper and lower boundaries for each element in the model and choose a good starting network using his knowledge of the DUT and its package technology.

The design problem can then be stated as follows: Obtain the element values of the network so that its transfer function is *as close as possible* to the prescribed transfer function $\boldsymbol{F}(\boldsymbol{p}, \jmath\omega)$ over the frequency range of interest $[\omega_l, \omega_u]$. This approach can be applied in our network modelling problem but the prescribed transfer function is given by a test engineer or derived from the given network topology.

7.4.2 A Typical Case Study

The load model of Figure 7.4 is chosen to demonstrate how a DUT input impedance might be modelled.

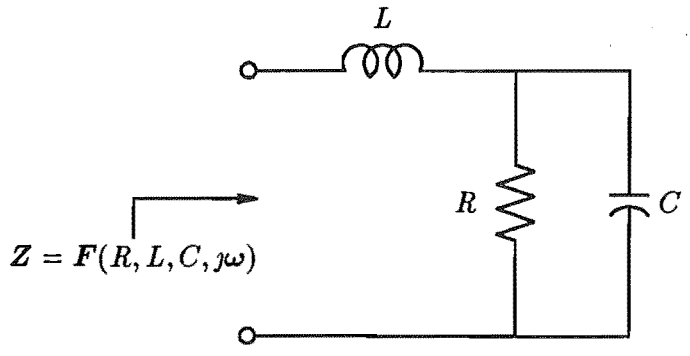


Figure 7.4 Circuit diagram of a typical DUT load.

The inductor L represents a bonding wire, or a conductor track, from a DUT package pin to a chip bonding pad. The value of L is chosen to be 5 nH as being typical for a DUT package. The 10 pF capacitor C represents stray and input capacitances at the DUT input pad. The 1 KΩ resistor R is the input resistance at the DUT input pad. A higher value of input resistance should be expected, for example for CMOS devices, but the sensitivity of the reflection coefficient decreases sharply for high resistor values. Therefore, the major contribution to the reflection coefficient would come from reactive elements, especially at high frequency.

In practice the prescribed frequency function $\boldsymbol{F}(\boldsymbol{p}, j\omega)$, is obtained by FDR measurement of the DUT at several discrete frequencies. The test engineer then chooses a linear network with a fixed topology whose component values are to be optimized to produce a matching frequency function. To test the optimization procedure, an actual linear network, with a topology as shown in Figure 7.4, is utilized to give predicted (rather than measured) characteristics at the sample frequencies.

This circuit topology will be used throughout the remainder of this work. The chosen component values are realistic estimates which remain fixed so as to verify the optimization performance for different initial conditions. They will not reflect all the actual values in practical use, since it is difficult to obtain a general representation of a DUT input for all technologies. In practice, the model element values or even the model itself may be unknown. Assuming that the user knows how to choose an appropriate model, this discussion shows how to obtain a "best fit" to the model, or in other words how to determine the model element values that give minimum error based on an error criterion of his choice.

The several reasons for using this specific circuit are listed below:

1. This circuit is a reasonable representation of a general load model for many DUTs (at least for first order correction for pulse integrity and time delay compensation).

2. Calibration time must be minimized for economic reasons. Several factors such as measurement time and computation time would contribute to lengthening the calibration time if a more complex model were used, and this is undesirable.

3. To help gain understanding during the development of multi-variable optimization methods, fewer than four variables should be used, since the human mind can visualize only three dimensions.

4. Once the concepts and techniques have been established, they can be extended to more complex load models. Most optimization algorithms have been well developed to handle multi-variable functions.

7.5 OBJECTIVE FUNCTION FORMULATION

To assign a more precise meaning to the phrase "as close as possible" (section 7.4.1), the design or test engineer may choose one of several error criteria in common use and

described in section 7.2.5.

7.5.1 Objective Function of the Example Circuit

$\widehat{\boldsymbol{F}}(\boldsymbol{p}, \jmath\omega)$ depends on the value of the network elements. A detailed description of the arguments in $\widehat{\boldsymbol{F}}(\boldsymbol{p}, \jmath\omega)$ is given by

$$\widehat{\boldsymbol{F}}(\boldsymbol{p}, \jmath\omega) = \widehat{\boldsymbol{F}}(R_1, R_2, \ldots, R_m; C_{m+1}, C_{m+2}, \ldots, C_n; L_{n+1}, L_{n+2}, \ldots, L_q; \jmath\omega) \tag{7.21}$$

assuming that the network under consideration is to be realized or to be modelled by resistors, capacitors, and inductors only. The resistors have been numbered from 1 to m, capacitors from $m+1$ to n, and inductors from $n+1$ to q. This means that the network has total of q elements as a combination of resistors, capacitors and inductors.

The problem is then to obtain the values of all the resistors, capacitors, and inductors such that $\boldsymbol{E}$ is minimized. To simplify the notation, let

$$\boldsymbol{p} \triangleq [R_1, R_2, \ldots, R_m; C_{m+1}, C_{m+2}, \ldots, C_n; L_{n+1}, L_{n+2}, \ldots, L_q]^T \tag{7.22}$$

In this example, the least $\mathcal{P}^{th}$ error criterion, described in section 7.2.5, is used to formulate the objective function $\boldsymbol{E}$ where

$$\boldsymbol{E}(\boldsymbol{p}, \jmath\omega) = \sum_{i=1}^{m} \left| \boldsymbol{W}_i \left(\widehat{\boldsymbol{F}}_i(\boldsymbol{p}, \jmath\omega) - \boldsymbol{F}_i(\jmath\omega) \right) \right|^{\mathcal{P}} \tag{7.23}$$

where m is the number of sample points chosen in the interval $[\omega_l, \omega_u]$. The number m depends on the functions $\widehat{\boldsymbol{F}}(\boldsymbol{p}, \jmath\omega)$ and $\boldsymbol{F}(\jmath\omega)$; if these functions are rapidly varying with ω, then the number of sample points, m, must be chosen to be large. If, on the other hand, these functions are relatively smooth, m is chosen to be small. However, choosing the number m large will increase both computation time and round-off error. Another problem, in our case, concerns the limited Pin Driver bandwidth. The minimum possible number of points m is the number of elements n in the network topology chosen by the test engineer.

For the example circuit, the objective function $\boldsymbol{E}$ was formulated using the following considerations:

- The number of sample points m, is chosen to be the minimum (i. e. $m = n = 3$).
- The desired responses $\boldsymbol{F}_i(\jmath\omega) = \boldsymbol{Z}_i(\jmath\omega); i = 1, \ldots, 3$ are obtained through analysis of the network at $\omega = \omega_i$.
- The responses, $\widehat{\boldsymbol{F}}_i^k(\boldsymbol{p}, \jmath\omega) = \widehat{\boldsymbol{Z}}_i^k(\boldsymbol{p}, \jmath\omega)$, at $\omega = \omega_i$ at the k^{th} iteration are computed according to

$$\widehat{\boldsymbol{Z}}_i^k(\boldsymbol{p}, \jmath\omega) = \frac{R_k}{1 + \omega_i^2 R_k^2 C_k^2} + \jmath\left(\omega_i L_k - \frac{\omega_i C_k R_k^2}{1 + \omega_i^2 R_k^2 C_k^2} \right) \tag{7.24}$$

- Two error functions, magnitude and phase, are formulated with $\mathcal{P} = 2$ (the least square objective function, equation 7.23). The total error is the sum of these two functions. Weighting factors, W_m and W_p, are used to give emphasis/deemphasis to the magnitude and phase errors respectively.

The minimum error of the least $\mathcal{P}^{th}$ type of objective function is known to be zero, if one can specify the exact values of the desired response. In practice, one could never reach this point, due either to computer roundoff and truncation error or inaccuracy in the measurement or calculation of the desired response. Therefore, error tolerance at the minimum point must be considered.

In the example circuit, the values of each element to give a global minimum is known. As will be seen later, this is a unimodal function. But, in practice, the test engineer will choose a circuit to represent a DUT or PEC receiver input impedance which may never yield an error value within the prescribed tolerance because either the circuit is inappropriate or there are significant errors in the target response obtained by measurement or calculation. For our development purposes, the errors in the target response are necessarily zero because the correct circuit is known.

A useful strategy for reducing computation time is to specify constraints in the form of upper and lower bounds on the acceptable range for each element in the circuit. In this example, the upper and lower bounds which define the feasible region are chosen as shown in Figure 7.5. The search for a minimum will take place only within these bounds.

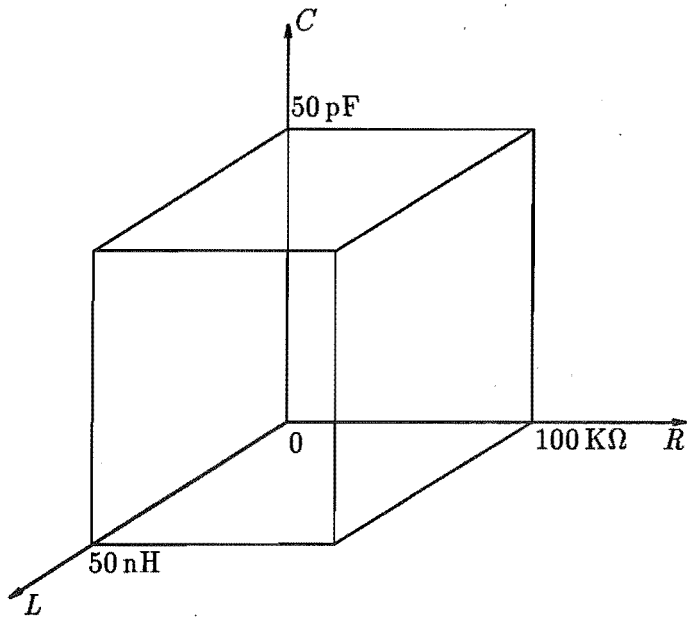


Figure 7.5 Upper and lower bounds for each element of the example load model.

The example then becomes a constrained optimization problem. Methods of trans-

forming a constrained problem into an unconstrained one have been discussed in section 7.2.4.

7.6 IMPLEMENTATION

The shape of the objective function depends upon the selected objective function formulation method. This will often determine the speed of the optimization process. Generally, one should try to avoid error shapes that lead to difficulties such as those shown in Figure 7.6.

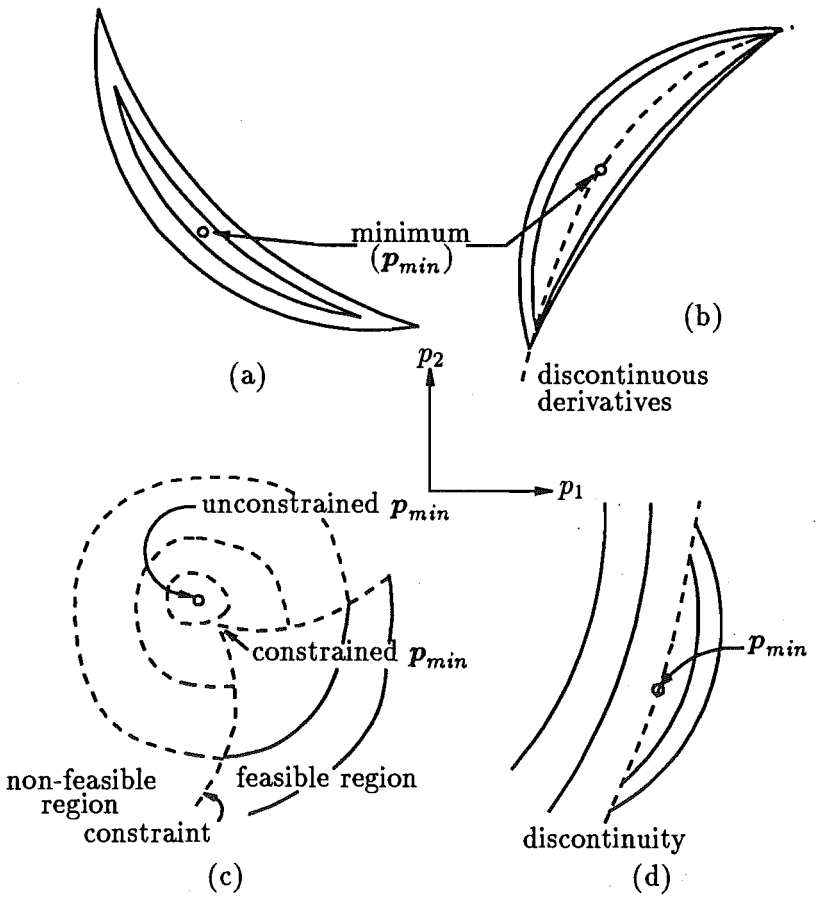


Figure 7.6 Contours which present difficulties to optimization strategies (a) a narrow curved valley (b) a narrow valley along which a path of discontinuous derivatives lies (c) a nonconvex feasible region (d) a discontinuous function.

In this example, the author chose an objective function formed by a least squares method, with weighting factors $W_m = 1$ and $W_p = 1$ (no emphasis or deemphasis). There may be other objective functions which yield better shapes than the selected one, but finding the best one is not a major objective at this stage.

The magnitude and phase of the example circuit are plotted from *d.c.* to 1 GHz, as shown in Figure 7.7. Assuming that the load reflection coefficients are measured at 100, 200 and 300 MHz, the error function can then be computed at these three frequencies.

Since there are three parameters in this case, a geometrical visual aid of the error function is not easily illustrated. However, Figures 7.8 to 7.11 give some surfaces ($\log(\boldsymbol{E})$ versus the parameters $\boldsymbol{p}$) and their corresponding contours for $R = 100, 500, 1000$ and $2000\,\Omega$. For higher values of resistor the error function is similar to that for $R = 2000\,\Omega$. Capacitor and inductor values are varied from 0 to 25 pF and 25 nH respectively.

As discussed in section 7.2.4, parameter transformation can be used to obtain an unconstrained problem. Using the transformation defined in equation 7.11, the parameters of the transformed vector $\acute{\boldsymbol{p}}$ are given by

$$\acute{p}_i = \cot \frac{\pi(p_i - p_{li})}{(p_{ui} - p_{li})} \tag{7.25}$$

However, from observation of the surface shapes of the selected objective function, this parameter transformation was not needed, because this function appears to be a unimodal function with only one global minimum within the defined feasible region. The error values become larger when they are remote from this minimum. To avoid the computational burden and truncation errors in such a transformation, the author chose not to use a transformation in this example. Only simple checks are employed to reject points lying in the absolute infeasible region (i. e. negative values).

7.6.1 Selection of an Optimization Algorithm

There have been many different methods proposed for defining the search direction $\boldsymbol{d}$. Two general classes of search direction procedures are:

1. *Direct search procedures* seek the minimum by evaluating only the objective function at successive trial points.

2. *Gradient search procedures* use not only the objective function but also the gradient $\partial \boldsymbol{E}/\partial \boldsymbol{p}$ and in some cases the Hessian $\partial^2 \boldsymbol{E}/\partial \boldsymbol{p}^2$. Gradient search methods generally require the determination of fewer trial points to converge to some prescribed neighbourhood of the minimum. On the other hand direct search methods require substantially fewer computations at each trial point $\boldsymbol{p}_i$. The complexity and requirements of a specific problem often determine the preferred algorithm.

More emphasis will be given to direct search methods than to gradient methods because they appear to have been more frequently used in network optimization. It may not be widely appreciated that most direct search methods are superior, in general, to the classical steepest descent method, and compare rather favorably with other gradient methods so far as efficiency and reliability are concerned [BANDLER, 1969].

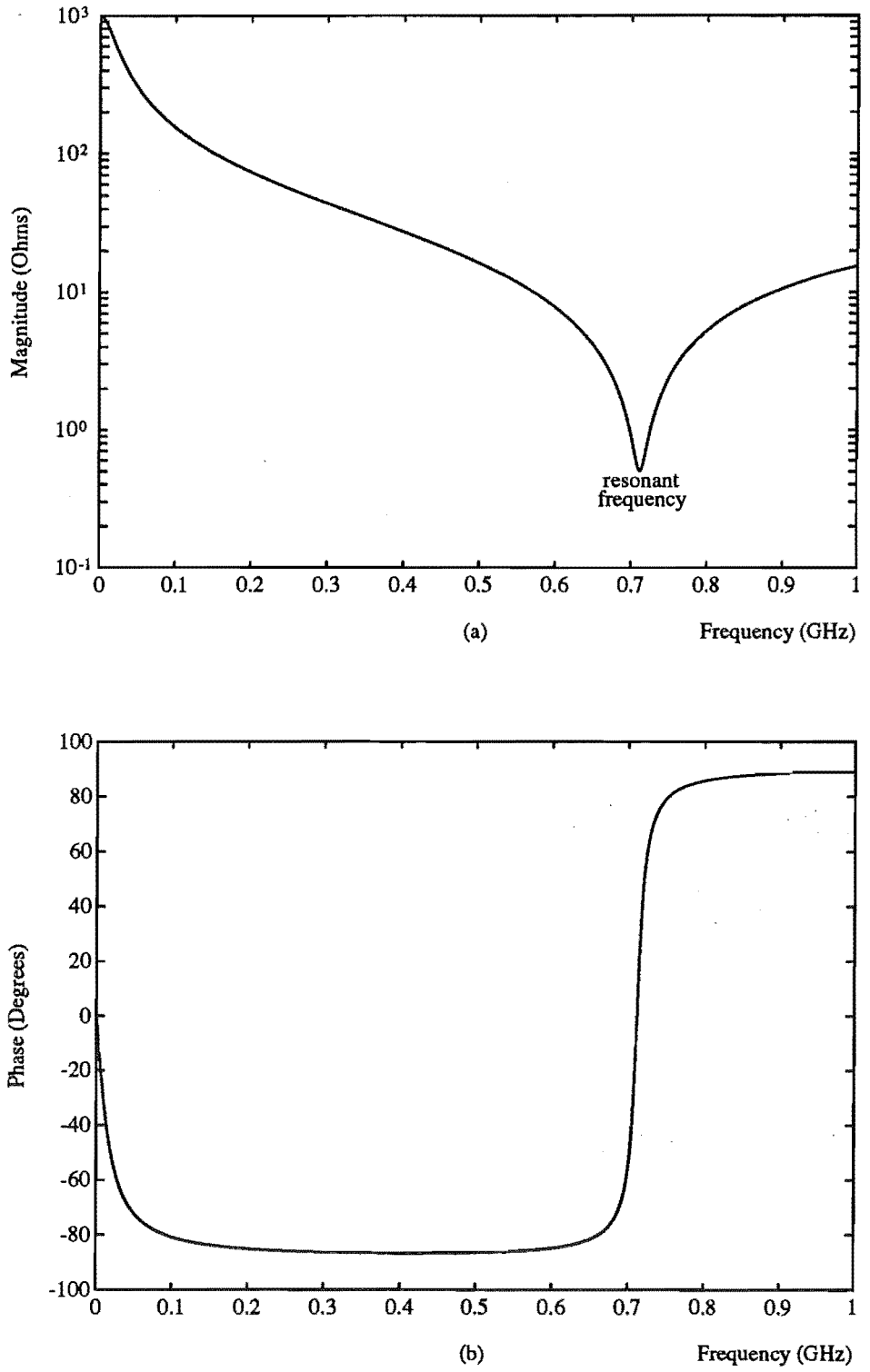


Figure 7.7 Frequency characteristic of the example load (a) Magnitude (b) Phase.

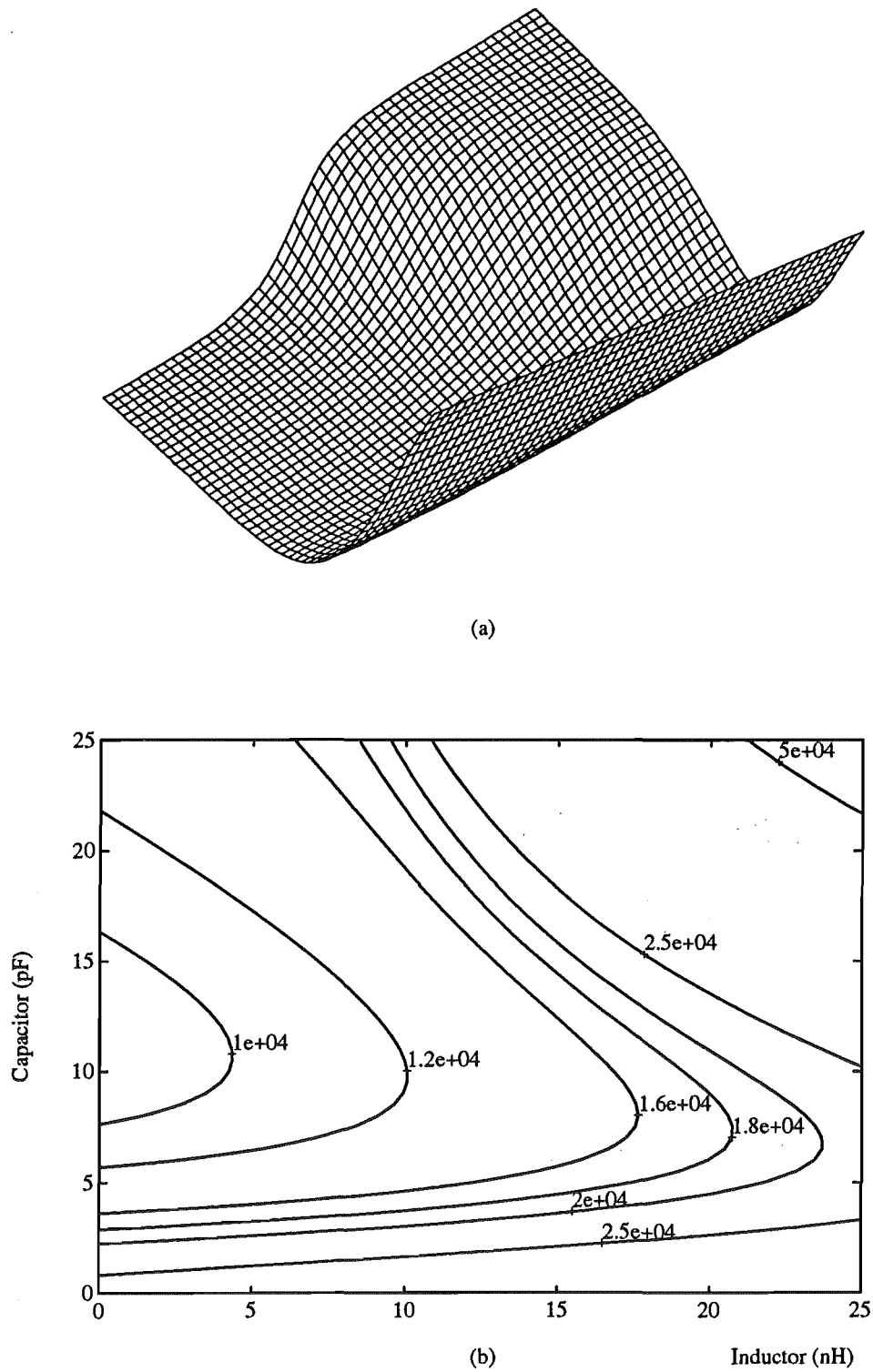
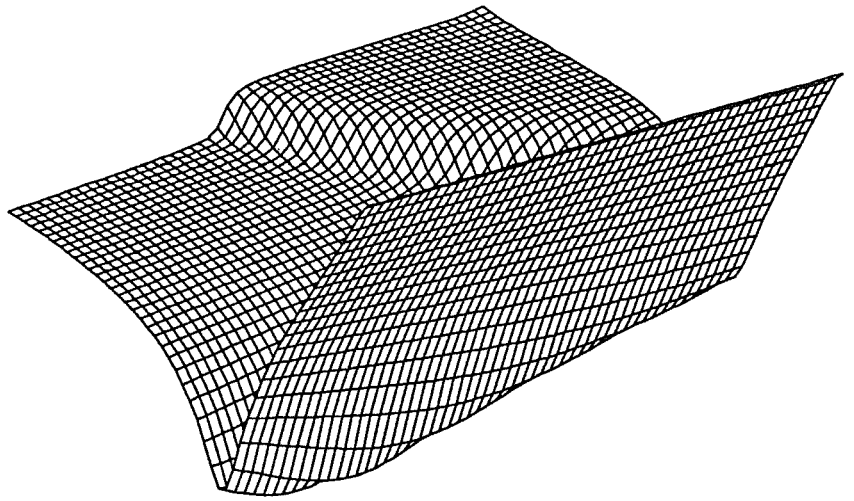
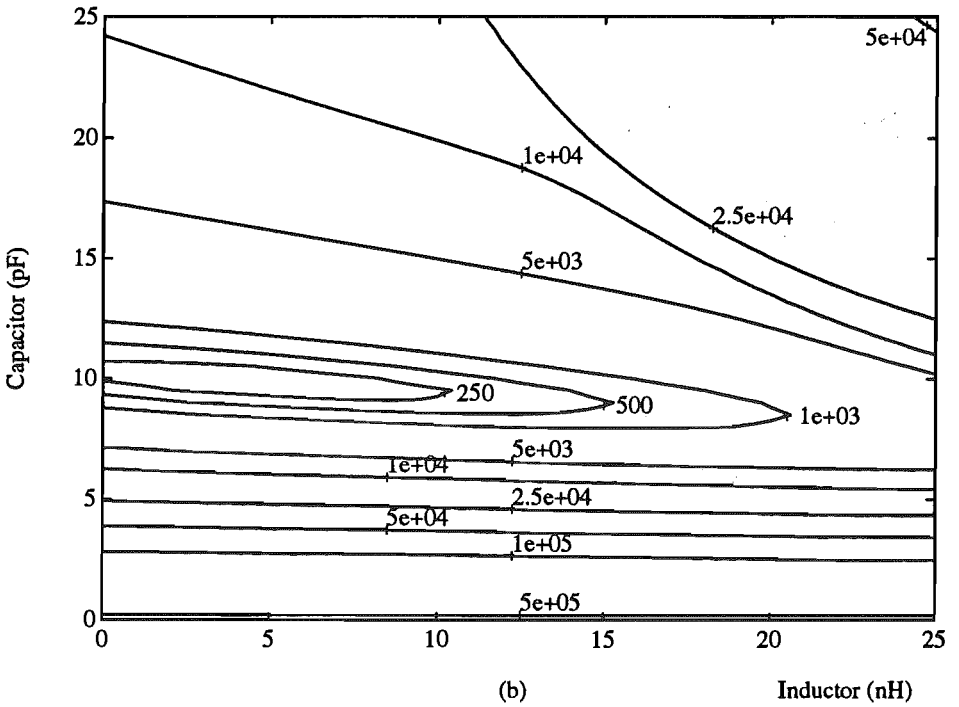


Figure 7.8 For $R = 100\,\Omega$ (a) surface representation of the error function (in log scale) (b) the corresponding contour.

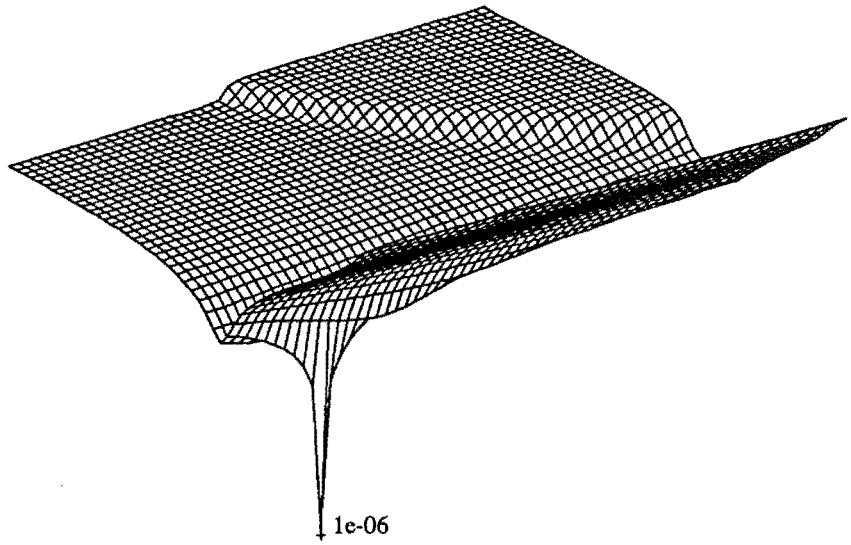


(a)

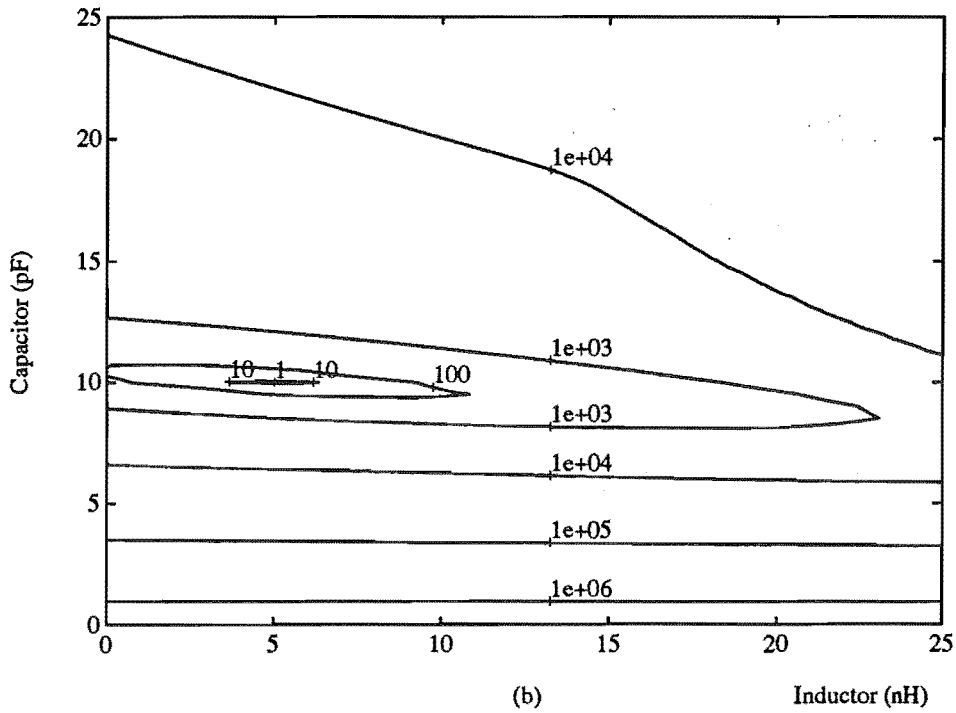


(b)

Figure 7.9 For $R = 500\,\Omega$ (a) surface representation of the error function (in log scale) (b) the corresponding contour.

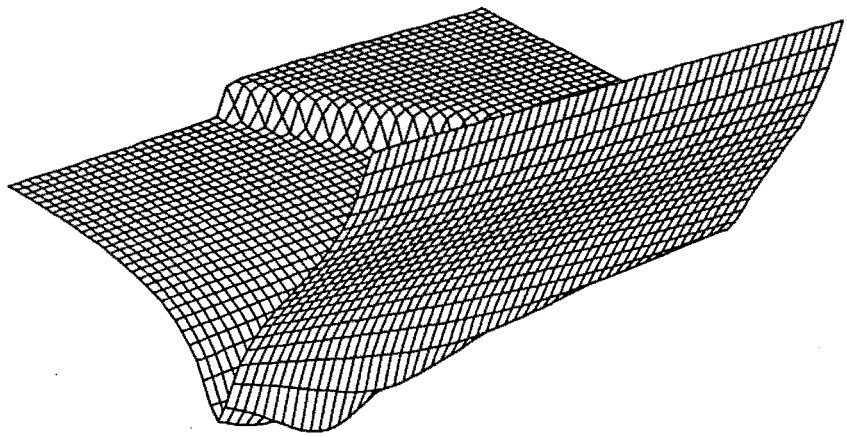


(a)



(b)

Figure 7.10 For $R = 1000\,\Omega$ (a) surface representation of the error function (in log scale) (b) the corresponding contour.



(a)

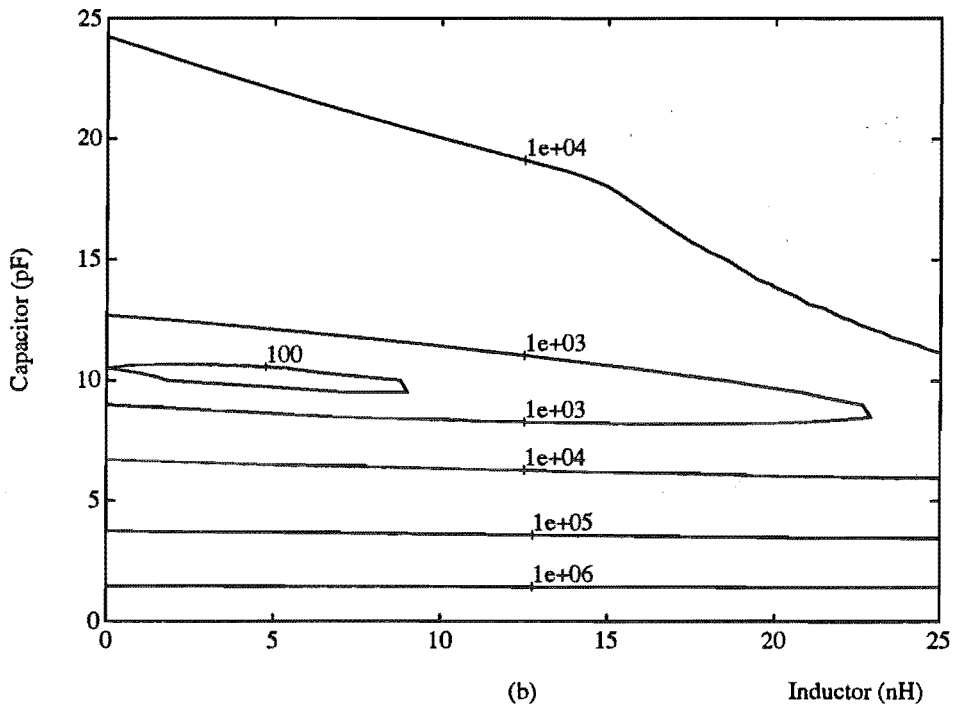


Figure 7.11 For $R = 2000\,\Omega$ (a) surface representation of the error function (in log scale) (b) the corresponding contour.

It is generally near the minimum that differences in efficiency between quadratically and nonquadratically convergent methods begin to manifest themselves. Besides, direct search methods are simpler to implement than gradient methods.

Two direct search methods were implemented; the simplex method [NELDER and MEAD, 1965] and pattern search [HOOKE and JEEVES, 1961]. Both programs were written, in C. Although these programs were customized for the example case, they should work for other moderately complex load models.

To apply these algorithms, one first creates a function which returns an error value, selecting terminating criteria and step-size parameters. These tasks, although apparently simple, demand a good understanding of the problem. Careful consideration must be given to the selection of both terminating and step-size criteria since they affect computation time.

Sections 7.6.2 and 7.6.3 describe the algorithms, based on the material from a paper by SORENSON and KOBLE [1976] and section 7.6.4 discusses how they were actually implemented.

7.6.2 The Nelder-Mead Simplex Method

The simplex method described here was developed by NELDER and MEAD [1965], and has been widely accepted as the best of the direct search methods [FIDLER and NIGHTINGALE, 1978]. The name simplex is taken from the topological generalization of a triangle. Just as a triangle is formed from a set of three points on a two dimensional surface, so in n-dimensional space a set of $n+1$ vertex points forms a simplex. For example, in three dimensions the vertices of a tetrahedron form a simplex. If all the points are equidistant from one another it is called a *regular simplex.*

The procedure involves the comparison of the values of the objective function at the $(n+1)$ vertices of a general simplex. Based on this comparison, a new simplex is generated and the comparison is repeated. The procedure involves three operations: reflection, expansion and contraction. In its most refined form, as suggest by NELDER and MEAD [1965], both the size and shape of the simplex are varied so that it can adapt itself to the local behaviour of the objective function. The optimization process may be visualised as the simplex tumbling about in error space, changing in size and shape in its quest for a minimum.

Before describing the procedure, we first define the notation and then proceed to describe the three basic operations.

Suppose that $(n+1)$ points, $\boldsymbol{p}_i; i = 0, 1, \ldots, n$, are given. We define $\boldsymbol{p}^H$ as the vertex which corresponds to the highest value of error $(\boldsymbol{E}^H)$, $\boldsymbol{p}^L$ as the vertex which corresponds to the lowest value of error $(\boldsymbol{E}^L)$, $\boldsymbol{p}^S$ as the vertex which corresponds to the second highest value of error $(\boldsymbol{E}^S)$. Let $\bar{\boldsymbol{p}}$ denote the centroid of all the points

except $\boldsymbol{p}^H$

$$\bar{\boldsymbol{p}} \triangleq \frac{1}{n} \sum_{\substack{i=0 \\ i \neq i^H}}^{n} \boldsymbol{p}_i \tag{7.26}$$

1. *The basic operations*

   (a) *Reflection*
   A reflection step is defined as

   $$\boldsymbol{p}^R \triangleq (1+\alpha)\bar{\boldsymbol{p}} - \alpha \boldsymbol{p}^H \tag{7.27}$$

   where $\alpha > 0$ is the reflection coefficient and will give the length of the reflection. NELDER and MEAD [1965] suggested that a suitable value for the reflection coefficient is $\alpha = 1$ but its value may be chosen by experiment.

   (b) *Expansion*
   An expansion step is defined to be

   $$\boldsymbol{p}^E \triangleq \gamma \boldsymbol{p}^R + (1-\gamma)\bar{\boldsymbol{p}} \tag{7.28}$$

   where $\gamma > 1$ is the expansion coefficient and it is also chosen arbitrarily, using experience as a guide, NELDER and MEAD [1965] suggested that a suitable value for γ is 2.

   (c) *Contraction*
   A contraction step has the same form as the expansion step, but the contraction coefficient β is between 0 and 1 (a reasonable choice is 0.5). This operation is defined as

   $$\boldsymbol{p}^C \triangleq \beta \boldsymbol{p}^H + (1-\beta)\bar{\boldsymbol{p}} \tag{7.29}$$

   Figure 7.12 (a) illustrates these three steps. The names of the steps should be evident from this diagram. The shrinking operation in Figure 7.12 (b) is performed when the reflection operation gives higher error than $\boldsymbol{E}^H$.

2. *The starting procedure*
   The choice of the starting simplex can affect the behavior of the procedure. Some procedures can be used to generate the initial simplex given a trial estimate $\boldsymbol{p}_0$. A commonly used one is [PRESS *et al.*, 1988]

   $$\boldsymbol{p}_i = \boldsymbol{p}_0 + \mu_i \boldsymbol{e}_i \tag{7.30}$$

   where $\boldsymbol{e}_i$ are n unit vectors, and where μ_i is a set of scaling factors in each direction which are selected depending on the problem's characteristic length scale.

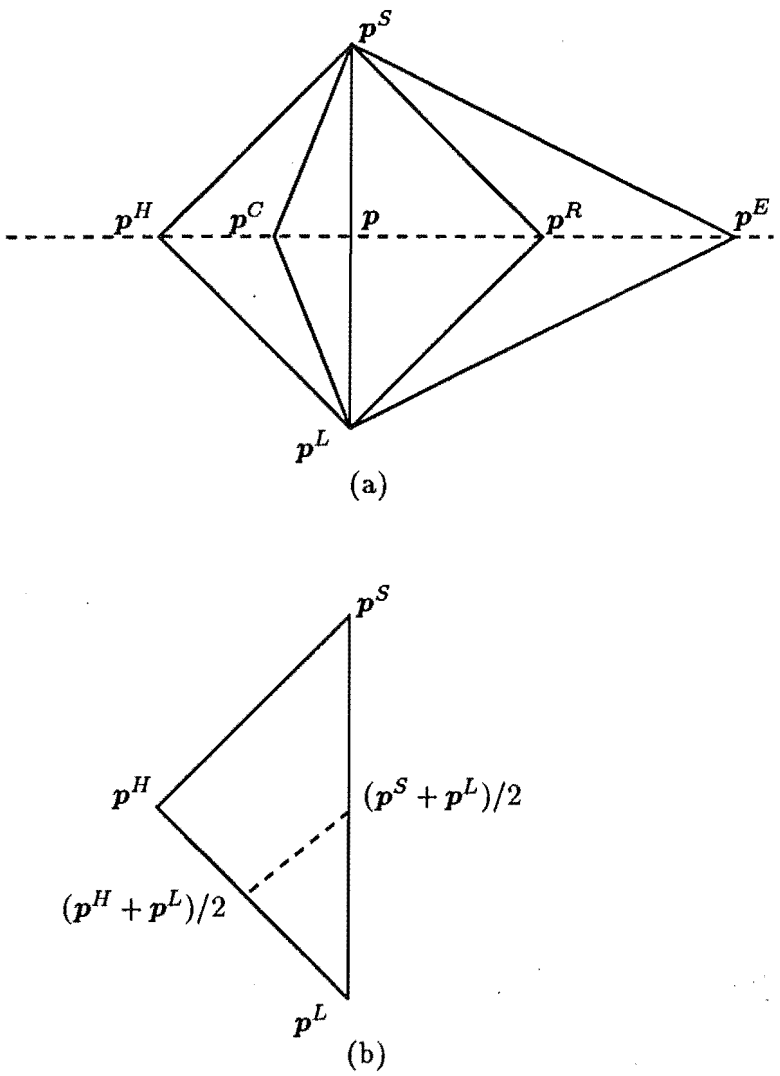


Figure 7.12 The Nelder-Mead simplex method (a) the three basic operations (b) the shrinking operation.

3. *Continuing the search*
   Suppose that we have prescribed α, γ, β, and the $(n+1)$ points $\boldsymbol{p}_0, \boldsymbol{p}_1, \ldots, \boldsymbol{p}_n$.

   (a) Determine $\boldsymbol{p}^H, \boldsymbol{p}^S, \boldsymbol{p}^L$ and $\bar{\boldsymbol{p}}$ and test for convergence

   (b) Take a reflection step to determine $\boldsymbol{p}^R$ using equation 7.27, then calculate $\boldsymbol{E}^R = \boldsymbol{E}(\boldsymbol{p}^R)$.

   (c) If $\boldsymbol{E}^H > \boldsymbol{E}^R \geq \boldsymbol{E}^L$, then replace $\boldsymbol{p}^H$ with $\boldsymbol{p}^R$.

   (d) If $\boldsymbol{E}^R < \boldsymbol{E}^L$, the reflected point has lower error function value than all other points in the simplex. We may therefore expand in what appears to be a favourable direction using equation 7.28 to yield $\boldsymbol{E}^E = \boldsymbol{E}(\boldsymbol{p}^E)$. If $\boldsymbol{E}^E < \boldsymbol{E}^R$, then replace $\boldsymbol{p}^H$ with $\boldsymbol{p}^E$. Otherwise, let $\boldsymbol{p}^R$ replace $\boldsymbol{p}^H$ and

return to step 3a.

(e) If $E^R > E^S$, only a slight improvement has been gained. In this circumstance we define p^H to be either p^H or p^R depending on which yields the smaller error value. Then the contraction step is taken in case a better point has been overshot. If the point p^C so obtained is such that $E^C = E(p^C) < E^H$, p^H is set equal to p^C, and the process is restarted from step 3a with the new simplex.

(f) If $E^R > E^H$, then no improvement has been gained from reflecting the simplex. The implication is that the minimum probably lies within the simplex. The simplex may therefore be shrunk about the point of the lowest error value E^L, by replacing all the other points in the simplex p_i by $\frac{1}{2}(p_i + p^L)$ and we return to step 3a.

4. *Ending the search*

The search continues until the simplex size is less than a specified amount, i. e. $p^H - p^L < \epsilon$. This indicates that a minimum point either local or global has been reached.

7.6.3 Pattern Search of Hooke-Jeeves Method

The basic pattern search takes incremental steps after suitable directions have been found by local exploration. If the search progresses well in terms of decrementing of the objective function, the step size is increased. If it is not progressing, either because the minimum is near or because of difficulties, such as a narrow valley, the step size is reduced. When the step size is reduced below a given value the search is stopped.

The search procedure devised by [HOOKE and JEEVES, 1961] consists of exploratory moves and acceleration or pattern steps, as shown in Figure 7.13. It is able to follow along narrow valleys because it attempts to align a search direction along the valley [BANDLER, 1969].

First, we define the two steps, and then the search procedure is described.

1. *Exploratory move*

The exploratory move consists of a collection of individual steps starting from some initial point p_{0k}. To begin, suppose that step-size parameters $s > 0$ have been defined. Let $i = 1$, and define an exploratory step as

$$p_{ik} \triangleq p_{(i-1)k} \pm s\, e_i \tag{7.31}$$

where e_i represents a coordinate vector

$$e_i \triangleq [0 \ldots 1 \ldots 0]^T \tag{7.32}$$

and it is the i^{th} component of e_i which equals one.

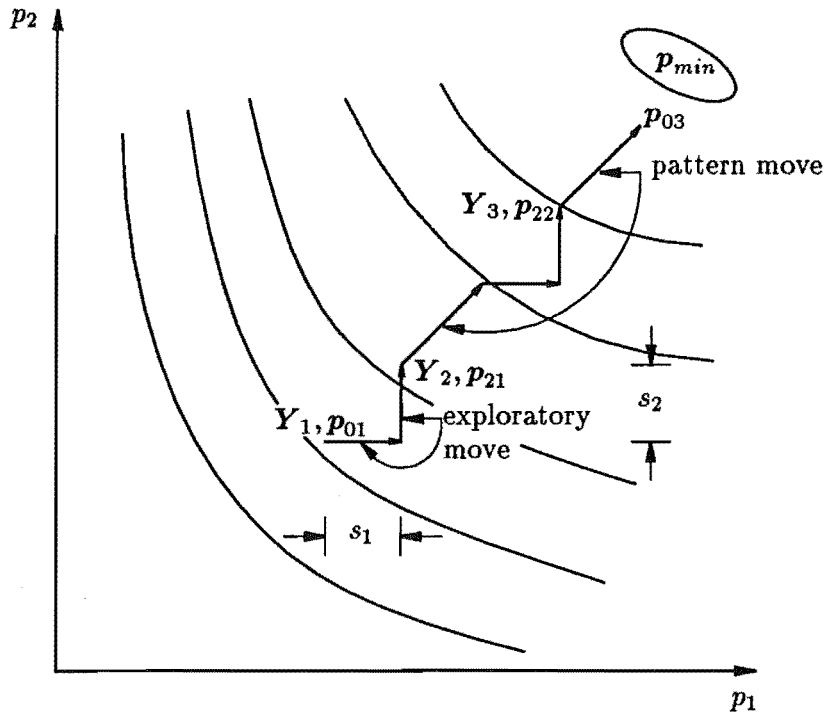


Figure 7.13 The exploratory and pattern moves of the pattern search algorithm.

Suppose we start by increasing p_i, using

$$p_{ik} = p_{(i-1)k} + s\,e_i \tag{7.33}$$

The step in equation 7.33 can have one of two possible results:

(a) If the objective function is reduced

$$E(p_{ik}) < E(p_{(i-1)k}) \tag{7.34}$$

then set $i = i + 1$ and return to equation 7.33.

(b) If the objective function is not reduced

$$E(p_{ik}) \geq E(p_{(i-1)k}) \tag{7.35}$$

then repeat the exploratory step using

$$p_{ik} = p_{(i-1)k} - s\,e_i. \tag{7.36}$$

The step in equation 7.36 can also have either of two results:

i. If the objective function is reduced (as in equation 7.34) then set $i = i+1$ and return to equation 7.33.

ii. If the objective function is not reduced (as in equation 7.35) then let

$$\boldsymbol{p}_{ik} = \boldsymbol{p}_{(i-1)k} \tag{7.37}$$

set $i = i + 1$, and return to equation 7.33.

The exploratory steps in equations 7.33, 7.36, and 7.37 are repeated for $i = 1, 2, \ldots, n$. This set of n steps produces s_{nk} and constitutes an exploratory move.

2. *Acceleration step*

Successive exploratory moves may produce a pattern as they often cause the search to follow a valley of the objective function. To make use of the information implied by successive exploratory moves, we define an acceleration step.

Let $\boldsymbol{Y}_i$ defines *base points* for the search procedure. Suppose that the base points $\boldsymbol{Y}_k$ and $\boldsymbol{Y}_{k+1}$ are given. Then an *acceleration step* is defined as the point $\boldsymbol{p}_{0(k+1)}$ where

$$\begin{aligned} \boldsymbol{p}_{0(k+1)} &\triangleq \boldsymbol{Y}_{k+1} + (\boldsymbol{Y}_{k+1} - \boldsymbol{Y}_k) \\ &= 2\boldsymbol{Y}_{k+1} - \boldsymbol{Y}_k \end{aligned} \tag{7.38}$$

Having defined the exploratory move and the acceleration step, we can now describe Hooke and Jeeves search procedure.

1. *Starting procedure*

Suppose that an initial base point $\boldsymbol{Y}_1$ has been prescribed and let

$$\boldsymbol{p}_{01} = \boldsymbol{Y}_1 \tag{7.39}$$

Perform an exploratory move and generate $\boldsymbol{p}_{n1}$.

(a) If $\boldsymbol{p}_{n1} = \boldsymbol{Y}_1$ then the step-size parameter is too large and must be reduced. Then, the exploratory move is repeated until one obtains a point $\boldsymbol{p}_{n1} \neq \boldsymbol{Y}_1$.

(b) If $\boldsymbol{p}_{n1} \neq \boldsymbol{Y}_1$, let

$$\boldsymbol{Y}_2 = \boldsymbol{p}_{n1} \tag{7.40}$$

and take an acceleration step (equation 7.38) to obtain $\boldsymbol{p}_{02}$.

2. *Continuing the search*

Suppose we have base points $\boldsymbol{Y}_k, \boldsymbol{Y}_{k-1}$ and $\boldsymbol{p}_{0k}$. Perform an exploratory move to generate $\boldsymbol{p}_{nk}$.

(a) If $\boldsymbol{E}(\boldsymbol{p}_{nk}) < \boldsymbol{E}(\boldsymbol{Y}_k)$, let

$$\boldsymbol{Y}_{k+1} = \boldsymbol{p}_{nk} \tag{7.41}$$

and perform an acceleration step to generate $\boldsymbol{p}_{0(k+1)}$.

(b) If $E(p_{nk}) \geq E(Y_k)$, let

$$p_{0k} = Y_k \tag{7.42}$$

and perform an exploratory move relative to Y_k. As a result of this move, we have two possible results.

i. If $E(p_{nk}) < E(Y_k)$, use equation 7.41 and perform an acceleration step to generate $p_{0(k+1)}$. Repeat the procedure for this trial point.

ii. If $E(p_{nk}) \geq E(Y_k)$ then the step-size parameter s is too large. Reduce s and repeat the exploratory move relative to Y_k.

3. *Ending the search*
The search continues until the step-size parameter is less than a specified amount. This indicates that the minimum has been located to within a neighbourhood defined by the lower bound prescribed for s.

7.6.4 The Actual Implementation

The source codes are not included since they are not suitable for present here. Instead, three flow charts are given; for the main program in Figures 7.14, for the simplex method in Figures 7.15, and for the pattern search in Figures 7.16.

7.6.4.1 The simplex method

Figures 7.15 shows the flow chart of the implementation of the simplex algorithm. This function returns TRUE when the minimum error obtained is less than the specified value, and FALSE when the simplex size is smaller than the prescribed value but the error obtained is higher or the number of function evaluations exceeds the selected limit.

An *initial guess point* p_0 is generally required by this algorithm although it needs $n+1$ points during the optimizing processes. The remaining n points can be computed using the given point and knowledge of the problem. A typical method to obtain the remaining points is that suggested in section 7.6.2. In this example, a simplex is built around $\pm 10\%$ of the guess value.

An error evaluation at the guess point is performed at this stage. If the error value is less than that prescribed in the terminating criteria then the program will stop and print out the optimum point obtained. On the other hand, if the error value obtained is too high (higher than a prescribed value, 10^5), then the error value is printed out and the initial point is rejected. The user is then asked for a new guess point. This is a very important step because the computation time depends strongly on the initial point, and will provide some indication to the user that the guess point is far away from a minimum.

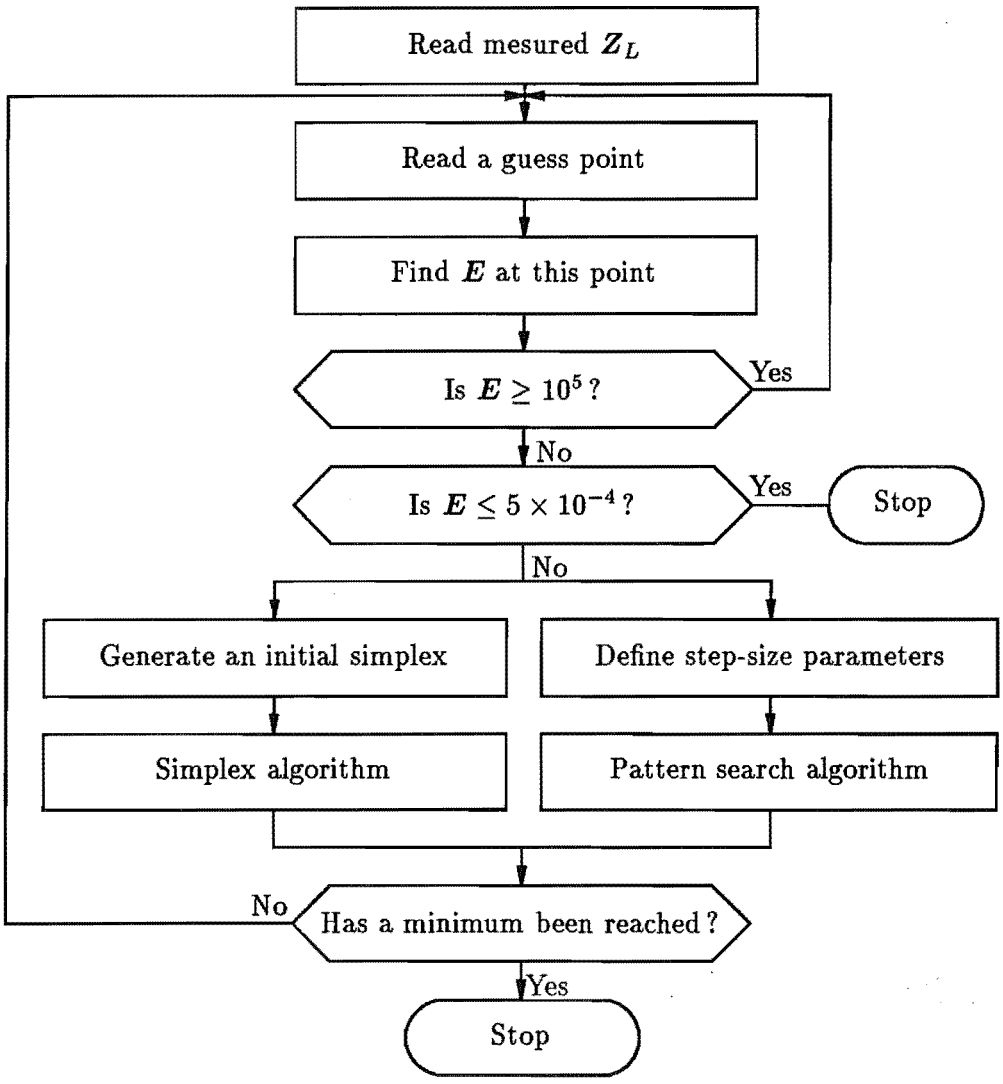


Figure 7.14 Flow chart illustrating the implementation of the main procedure.

The reflection, expansion, and contraction coefficients were chosen to be 1.0, 2.0 and 0.5 respectively. The simplex procedure and some utilities are taken from the book *Numerical Recipes in C* by PRESS *et al.* [1988].

Termination criteria must be carefully chosen because in practice we have no prior knowledge of the minimum error value. It could be very high if the chosen model does not properly represent the actual load. Although theoretically the minimum value of the least squares method is known to be zero, in practice this value is rarely achieved for reasons discussed in the previous section.

In this implementation, three different criteria are used to terminate the optimization procedure.

- The maximum number of objective function evaluations for each iteration is 1000, to prevent unnecessary computation when the program does not converge within

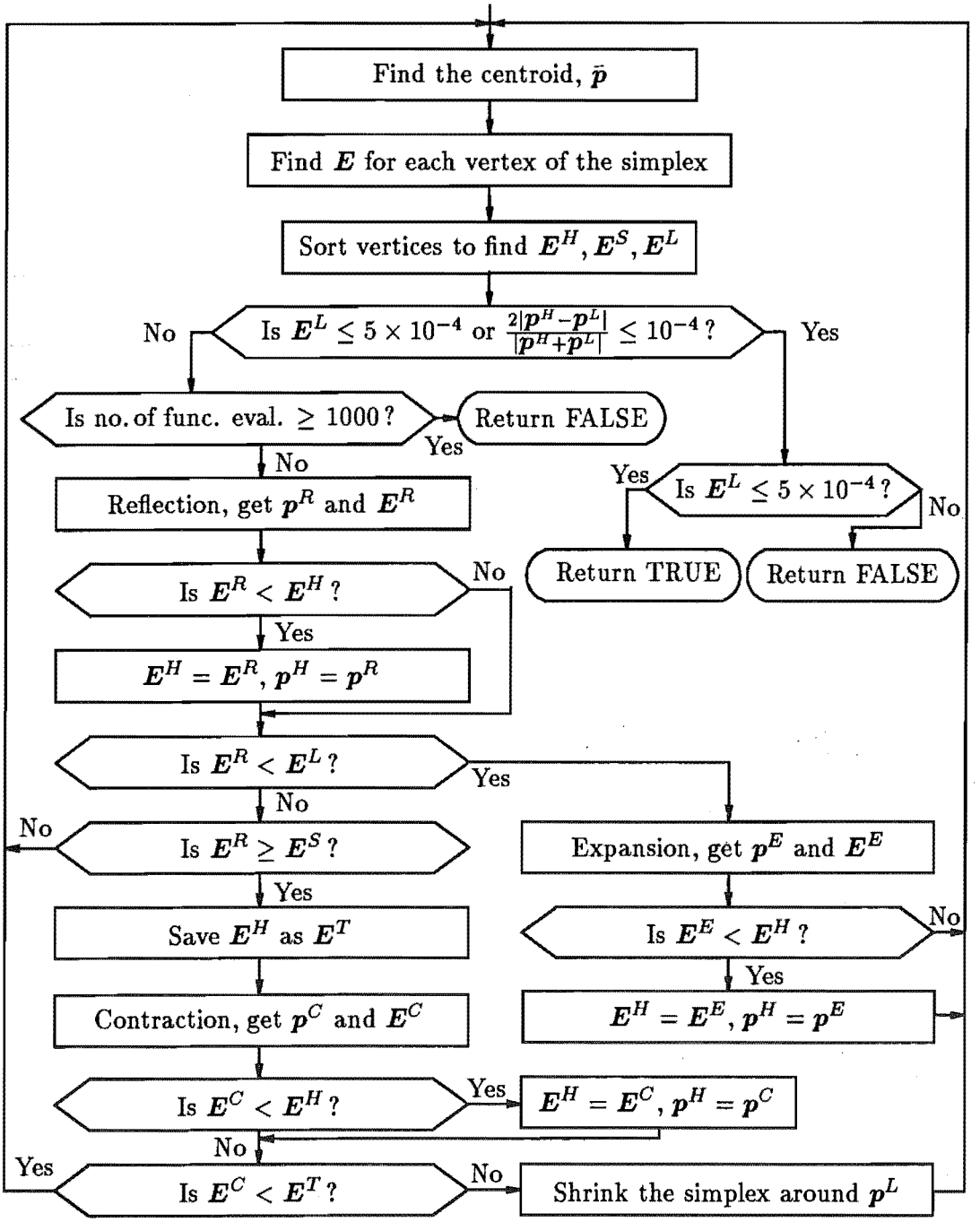


Figure 7.15 Flow chart illustrating the implementation of the simplex method.

the specified number of function evaluations. The user can restart the procedure using either the lowest error value from the last iteration, or he may select a new initial point.

- The distance between the highest error value and the lowest error value is used to check whether the simplex size is smaller than a prescribed value. In the case where the simplex size is quickly reduced within a small number of function evaluations because the error surface is flat, the program may not find a minimum point. Another problem, called *degeneracy*, in which the simplex is degenerated into a subspace of dimensions less than $n + 1$, may occur and one must then restart with a new simplex.

- The size of the simplex does not guarantee that a minimum has been reached. The target value of the objective function is used as an indication of success, and is set at 5×10^{-4} for our particular case. Choice of this value is very dependent on how the objective function was formulated. Hence, one must be very careful when selecting it. In practice, its value can be set higher and the optimization procedure can be run to see if it can reach this point. If successful, a smaller value may be used instead. In this way, one can avoid setting an impossible target.

  Once this criterion has been satisfied, one can be certain that the acceptable minimum point has been reached and the program will then print the parameter values.

7.6.4.2 The pattern search method

Figure 7.16 shows the pattern search algorithm flow chart. This function returns TRUE when the minimum error obtained is less than the specified value and FALSE when all the step-size parameters are smaller than the prescribed values but the error obtained is higher or the number of function evaluations exceeds the selected limit.

A guess point is required for this algorithm, and an error evaluation is performed on the given point in a similar manner to that in the previous method. The critical parameter is the step size, both for starting and ending the search. It generally takes a longer time to converge if the starting step size is too large, or too small. The starting step size parameters have been chosen to be $100\,\Omega$ for a resistor, 1 pF for a capacitor, and 0.5 nH for an inductor. However, if the given $R \geq 6000$ the starting step size is changed to $1000\,\Omega$. Similarly, if the given $L \geq 10$ nH the starting step size is changed to 1 nH and if the given $C \geq 20$ pF the starting step size is changed to 2 pF.

The ending step-size parameters have been chosen to be $0.01\,\Omega$ for a resistor, 0.001 pF for a capacitor, and 0.001 nH for an inductor. These final step sizes may not guarantee a global minimum, so the error value is again used to ensure the obtained minimum is acceptable.

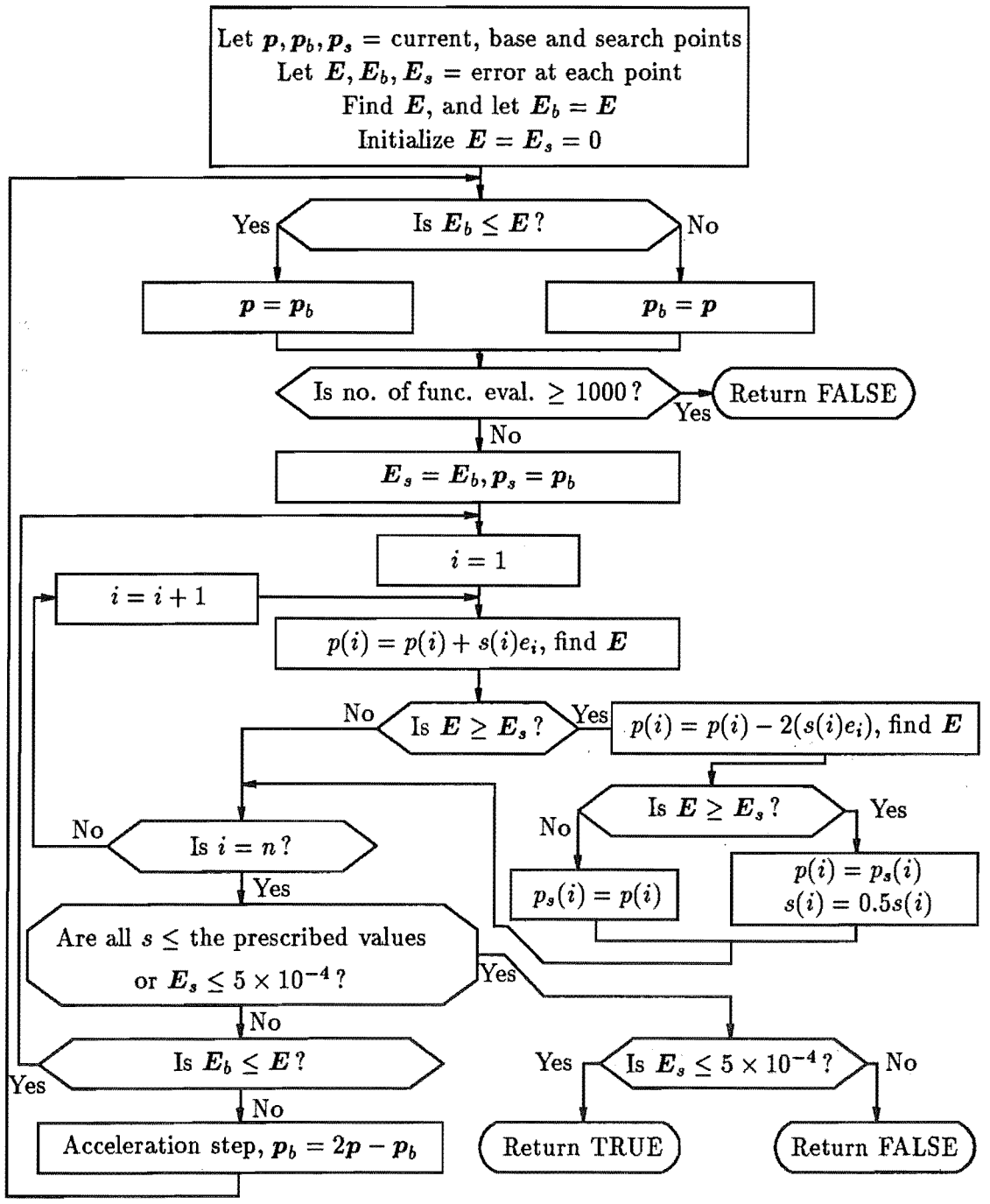


Figure 7.16 Flow chart illustrating the implementation of the pattern search method.

If the program cannot find a better point in an exploratory move, the step size is reduced by half.

In the pattern search procedure described above, a point generated by a pattern move is not evaluated and then compared with the current base point, but another exploratory move is performed around this point. If there is any better point then the program will move the base point to that point, if not it will use the current base point and start the search again. In this implementation, a point generated by a pattern move is evaluated and compared with the current base point. The program will take the lower error value as a new base point. This method gives results similar to those obtained using the basic procedure. The exploratory and pattern moves of the actual implementation are depicted in Figure 7.17. Note that the program reaches p_{03} in 6 steps which is the same as that shown in Figure 7.13. The difference is that there is only one iteration in Figure 7.13 but there are two iterations in Figure 7.17.

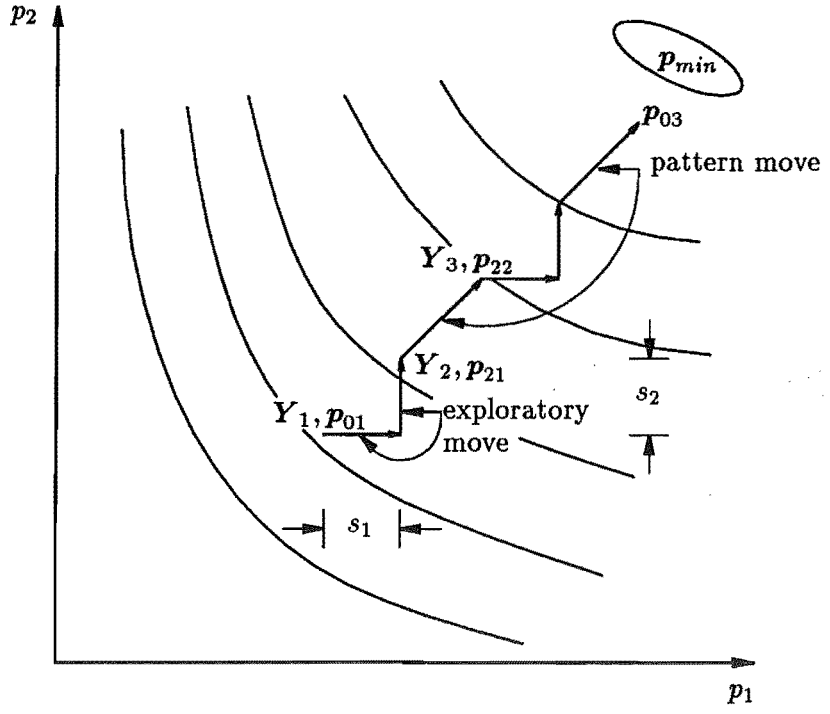


Figure 7.17 The exploratory and pattern moves of the pattern search algorithm in the actual implemetation.

7.7 RESULTS FOR THE EXAMPLE CASE

The programs have been tested on the example circuit with different initial points. Both algorithms give satisfactory results when the initial trial point is within the feasible region. A small problem occurs only when the resistor value of the guess point is high

(i. e. more than 10 KΩ), when the program takes a long time and results in high number of function evaluations. This is because the sensitivity to resistor variation is very low at high resistor values, and the error surface appears to be nearly flat at this end.

To aid comparison, 20 initial points are used to demonstrate the performance of both programs. The results are tabulated in Tables 7.1 and 7.2. The number of function evaluations is compared rather than the number of iterations, because iterations in the programs are different. This should give a more direct comparison, since most of the computation time is employed evaluating the objective function.

Case	Starting point			Ending point					
				Simplex			Pattern		
	R(Ω)	L(nH)	C(pF)	R(Ω)	L(nH)	C(pF)	R(Ω)	L(nH)	C(pF)
1	2500	6	12	1001	4.996	10	1000	5	10
2	525	12.9	15.2	1000	4.9909	10.001	999.6	5.0094	9.9988
3	7560	2.7	6.9	1000	5.0089	9.9991	1001	4.9969	10.001
4	278	15.4	13.1	1000	5.0111	9.9996	999.9	5.0094	9.9984
5	12345	7.8	21.4	1001	4.9921	10.001	1001	4.9953	10.001
6	610	22.6	17.7	1000	4.995	10	1001	5.0062	9.9988
7	1230	3.2	5.8	1000	4.9951	9.9997	1000	4.9969	9.9992
8	875	25.1	9.5	1001	4.9971	10.001	1000	4.9906	10.001
9	22000	4.8	13.6	2.4×10^4	5.1649	10.087	1000	5.0031	9.9994
10	55555	3.9	8.2	4.9×10^4	4.2842	10.166	999.8	4.9937	10.001
11	120	9.1	11.1	999.4	5.0081	9.9988	999.7	5.0062	9.9994
12	3695	17.7	32.3	1001	5.001	10.001	999.7	4.9969	10.001
13	467	2.2	14.8	1000	5.003	9.9986	999.8	5.0086	9.9992
14	996	4.4	9.2	1001	5.0014	10.001	1001	4.9937	10.001
15	1004	5.3	10.6	999.3	4.993	10	999.3	5.0031	9.9994
16	9999	1.5	28.3	999.4	3.0078	10.179	1001	5	9.9992
17	45	8.9	15.5	1001	4.9993	10	999.7	5.0094	9.999
18	358	0.4	7.7	999.5	4.9916	10.001	999.4	5.0094	9.9988
19	774	13.6	1.8	This trial point is rejected					
20	994	7.6	35	999.2	4.9969	10.001	1000	5.0063	10

Table 7.1 Performance comparison between simplex and pattern search methods; starting and ending point.

Case	Minimum error		Function evaluations		Comments
	Simplex	Pattern	Simplex	Pattern	
1	1.3773×10^{-4}	1.01673×10^{-6}	174	65	
2	2.6674×10^{-4}	3.2337×10^{-4}	146	108	
3	2.6758×10^{-4}	2.8005×10^{-4}	189	111	
4	4.8213×10^{-4}	4.5616×10^{-4}	133	117	
5	4.3658×10^{-4}	2.5955×10^{-4}	191	139	
6	7.3024×10^{-5}	3.6086×10^{-4}	117	143	
7	3.0293×10^{-4}	4.6743×10^{-4}	95	109	
8	2.8992×10^{-4}	2.4102×10^{-4}	146	145	
9	114.4	7.3668×10^{-5}	53	155	Simplex fails
10	118.7	1.2141×10^{-4}	46	368	Simplex fails
11	2.9053×10^{-4}	1.3715×10^{-4}	139	119	
12	2.5148×10^{-4}	3.0652×10^{-4}	189	198	
13	4.7839×10^{-4}	2.359×10^{-4}	113	159	
14	4.1664×10^{-4}	1.6633×10^{-4}	68	103	
15	2.8278×10^{-4}	1.0966×10^{-4}	135	111	
16	11.54	4.2653×10^{-4}	182	159	Simplex fails
17	8.3113×10^{-5}	2.9022×10^{-4}	156	118	
18	2.3026×10^{-4}	3.4072×10^{-4}	140	105	
19	–		0	0	Rejected with $E = 3.1232\times10^{5}$
20	3.2479×10^{-4}	2.1477×10^{-4}	125	172	

Table 7.2 Performance comparison between simplex and pattern search methods; minimum error and number of function evaluations.

From the comparisons, both algorithms give similar performance in terms of the number of function evaluations. For cases 9, 10 and 16, where the simplex method failed to converge, the initial resistor value is high. The reason is that the simplex size reduces quickly because the error surface around the guess point is flat. However, the end point obtained can be used as a new guess point and all of these cases converged at the second attempt.

The trial point for case 19 was rejected because the error value evaluated at this point was higher than 10^5. This is because the error surface is most sensitive to the variation of the capacitor value, resulting in significantly increased error values when

this element is varied from its minimizing point, as shown in Figures 7.8 to 7.11.

Two other interesting cases are 14 and 15, where the given trial points were deliberately chosen very close to the correct values. Both algorithms still need a considerable number of function evaluations to satisfy all the terminating criteria. Although the programs check the error value at the given point before calling the optimization procedure, this error value is still higher than the prescribed acceptable value, indicating that the error falls very sharply near the minimum, and this behaviour can be seen in Figure 7.10.

7.8 CONCLUSION

The reflection coefficients obtained from FDR measurements can be used to determine a load model. The models considered in this research are linear time-invariant networks which contain only a combination of resistors, capacitors and inductors.

The model parameters can be obtained through the use of appropriate optimization algorithms. Two algorithms, the simplex and pattern search, were implemented. Both methods, which are direct search methods, give satisfactory results. Their performances in terms of speed are similar.

CHAPTER 8

COMPENSATION TECHNIQUE

This chapter describes a technique to obtain compensation waveforms from channel and load characteristics. A theory of compensation and some practical limitations are discussed in sections 8.1. Details of element models in the transmission path between a PEC and a DUT pin are given in section 8.2. The proposed technique to compute a compensation waveform and a possible means to obtain an approximated compensation are next presented in section 8.3.

Two example cases are considered to demonstrate the proposed technique; matched and mismatched channels. Simulation results, for each case, obtained from the proposed compensation scheme are presented in section 8.5. Section 8.6 discusses the improvement in waveform quality and timing accuracy gained from this method.

8.1 COMPENSATION AND SOME LIMITATIONS

This section briefly addresses some difficulties in determining the transient response of a high speed digital system which consists of lossy distributed transmission line network and lumped nonlinear circuits, then describes basic concepts to compute a compensation for a linear system and how this technique can be applied in our application. Although the technique described in this thesis must be applied to a slightly lossy transmission line system, the discussion in this chapter considers *only* lossless transmission lines on the grounds that small losses are a minor purterbation that do not invalidate the major conclusions of a lossless analysis.

8.1.1 Transmission Path Terminated with an Arbitrary Load

The fundamental difficulty encountered in integrating transmission line simulation in a transient circuit simulator arises when circuits under consideration contain lossy transmission lines terminated with nonlinear loads. The nonlinear terminations must be characterized in the time domain while transmission lines with losses, dispersion, and interconnect discontinuties are best simulated in the frequency domain [WINKLESTEIN *et al.*, 1991]. Techniques for simulating such systems have recently been reviewed

[DJORDJEVIC *et al.*, 1987; BLAZECK and MITTRA, 1991].

There are two ways to simultaneously analyze the transmission line and the terminal networks. One way is to incorporate the analysis of the terminal networks into the analysis of the transmission line. For this approach one has to know, at each time instant, the equivalent parameters of the terminal networks, as seen from the transmission line. The other way is to incorporate the analysis of the transmission line into the analysis of the terminal networks. For this approach one has to know the instantaneous parameters of the transmission line, as seen from the terminal networks. The second approach is more effective because the transmission line is a linear network, which can be completely characterized in the time domain by its impulse response or Green's functions, but the terminal networks can be either linear or nonlinear. The Green's functions can be obtained from the frequency domain analysis such as Y-parameters [DJORDJEVIC *et al.*, 1987] or S-parameters [SCHUTT-AINE and MITTRA, 1988; WINKLESTEIN *et al.*, 1991]. The total response is then obtained through time domain convolution.

8.1.2 Effects of a Nonlinear Load

An element in the path which is likely to be nonlinear is the load at both ends of the transmission path (i. e. DUT or PEC receiver input impedances). The transmission path considered in this research is represented as a linear system with the load approximated as a linear time-invariant circuit.

To illustrate the nonlinear effects in a typical load, a circuit simulation such as SPICE can be used. In SPICE version 2G.6, only a lossless transmission line model is available. Although a lossy line can be modelled with a number of sections of lumped elements (each section represents an elemental section of the transmission line), this approach is cumbersome and is not necessary at this stage. The time domain Green's function obtained from S-parameters is preferable because Y-parameters have a wide dynamic range problems which may affect the computational stability and efficiency [WINKLESTEIN *et al.*, 1991].

Figure 8.1 shows a typical CMOS input protection circuit [BAKOGLU, 1990]. The circuit used in the simulation is illustrated in Figure 8.2. The nonlinear load (DUT) consist of the input protection circuit and a CMOS inverter which is terminated with a capacitive load C_L. The resistor R in Figure 8.1 (a) is split into two series resistors, R_1 and R_2 together with parasitic diode (D_5) from p+ to N WELL. The input pad is represented with a linear capacitor C_{Pad} and a diode D_{Pad} which represents N WELL to P substrate parasitics. The SPICE input file, which describe the devices' models and other parameters in the circuit, is given in appendix G.

Comparison of waveforms when the transmission line is terminated with only a linear capacitor C_{Pad} and that including the nonlinear load of Figure 8.2, is depicted in Figure 8.3.

Simulation results show that the nonlinear effects introduce minimum timing error at 2.5 V. This is because of the symmetry of the protection circuit, causing reverse

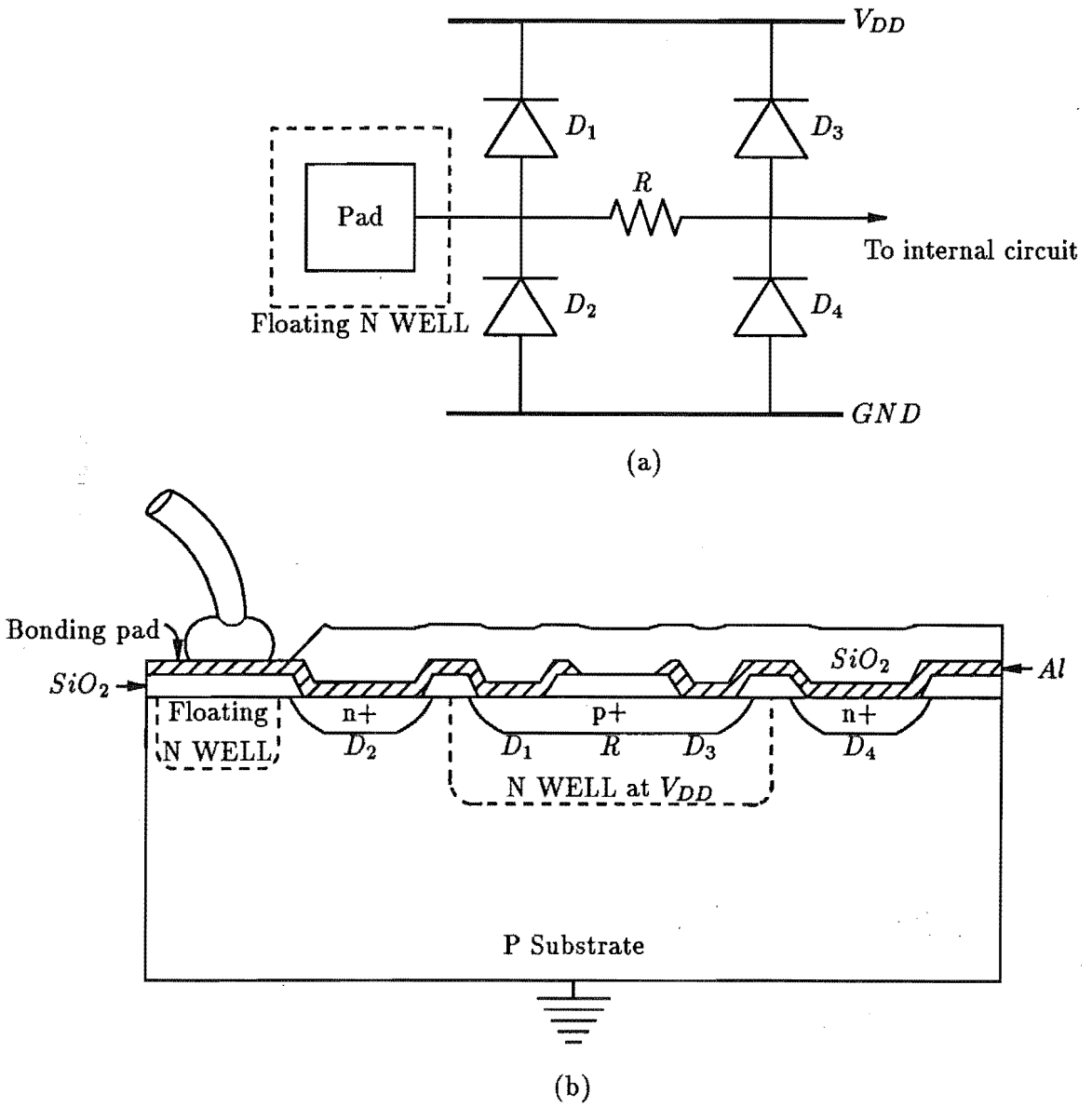


Figure 8.1 A typical input protection of CMOS devices (a) circuit diagram (b) wafer cross section.

biased junction capacitances to deviate minimally at this voltage level. This minimum capacitive load can be measured using the FDR facility described in the previous chapters. A small signal is employed in the FDR measurement, and if the signal is small enough so that the nonlinear capacitance can be approximated linear, the method described next should compensate for this timing error.

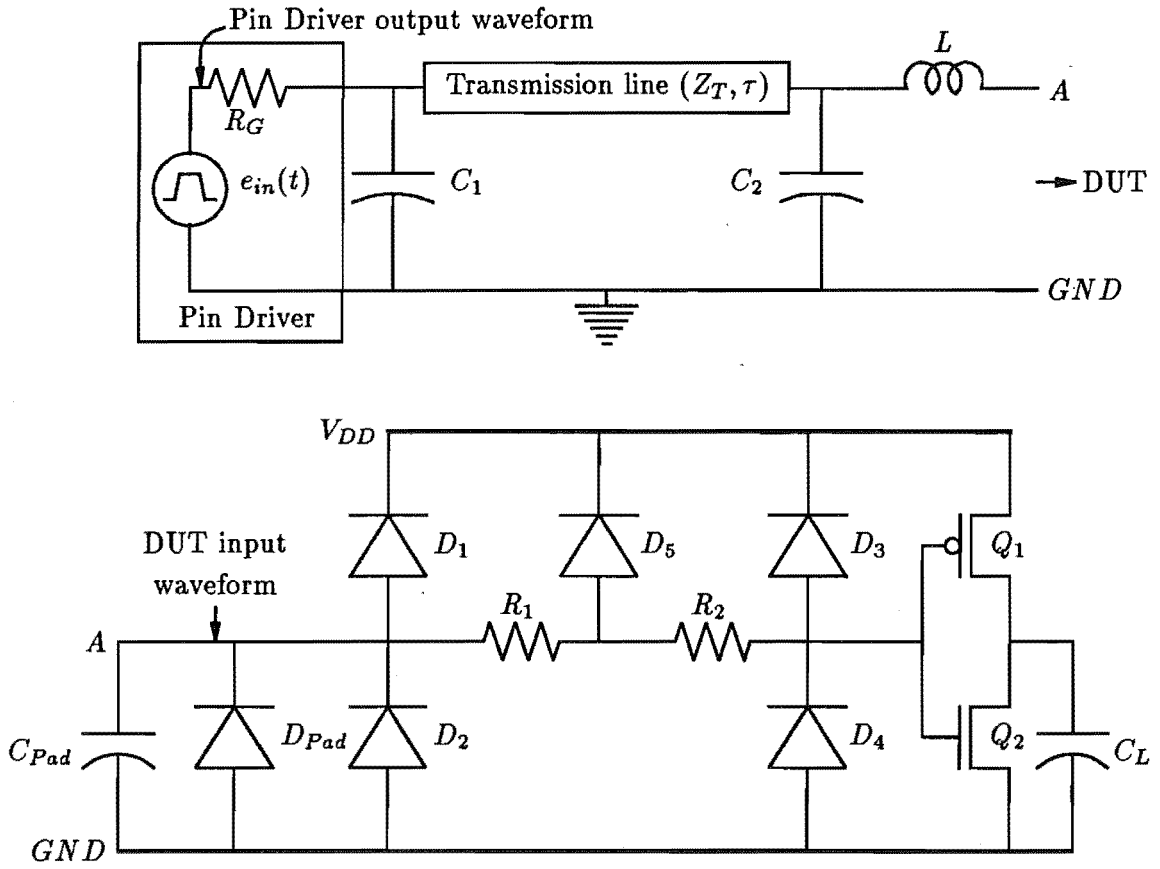


Figure 8.2 Circuit for SPICE simulation of the effects of a nonlinear load.

8.1.3 Compensation for a Linear Channel

A theory of compensation for a signal travelling through a linear channel or linear system, as illustrated in Figure 8.4, is simple to derive. For notational convenience, the complex frequency, $s = \sigma + j\omega$ will be used to describe some functions of frequency.

If the transfer characteristic of that system or channel is known to be $H(s)$, a compensation $E_{com}(s)$ required at the input of the system will be the difference between the input to the system and the output from the system divided by the system transfer function and can be written as

$$\begin{aligned} E_{com}(s) &= \frac{(E_{out}(s) - E_{in}(s)H(s))}{H(s)} \\ &= \frac{(1 - H(s))E_{in}(s)}{H(s)} \end{aligned} \tag{8.1}$$

In this case, the output will be the same as the input when $E_{in}(s) + E_{com}(s)$ is fed at the input of the system. Ideally, the signal must be compensated continuously over the frequency range of interest. The concept may be simple from theoretical point of

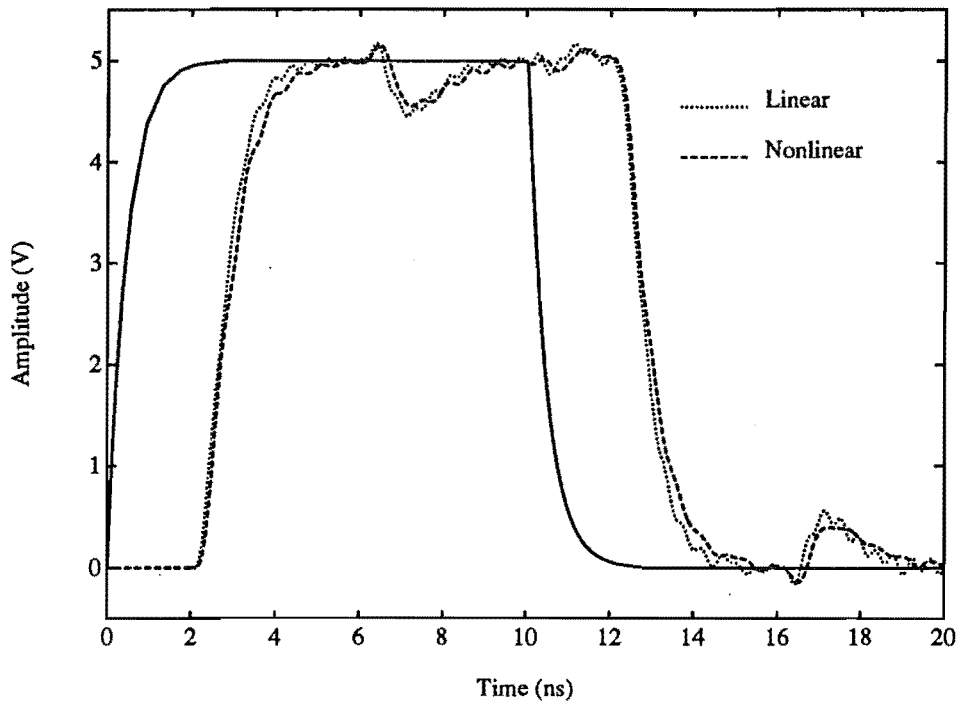


Figure 8.3 The SPICE simulation result on nonlinear effects.

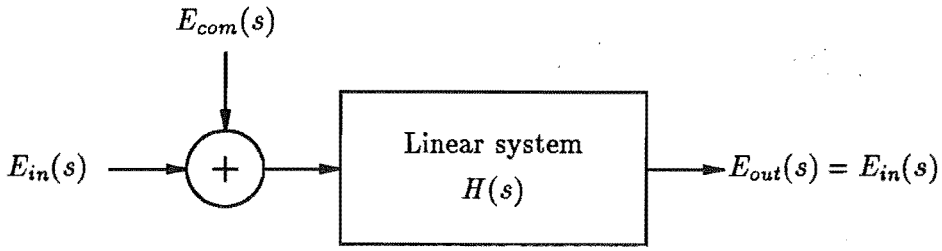


Figure 8.4 A compensation theory for a linear system.

view. However, in most cases, this is not practical due to difficulties in generation of the exact compensation over that frequency range especially for a computer-controlled system. A time domain compensation is more attractive if the compensation waveform can be easily generated. The time domain compensation, $e_{com}(t)$, can be obtained from the inverse Laplace transform of the frequency domain compensation, $E_{com}(s)$.

$$e_{com}(t) = \mathcal{L}^{-1}[E_{com}(s)] \tag{8.2}$$

The steps to compute a compensation waveform are summarized as follow:

1. Find the system transfer function.

2. Compute $E_{com}(s)$ for a given input $E_{in}(s)$ using equation 8.1.

3. Take the inverse Laplace transform to find the time domain waveform, $e_{com}(t)$.

8.1.4 Compensation When Driving a DUT

The input to this system is from a Pin Driver output, and the output goes to a DUT input. The ideal situation is to obtain a DUT input waveform identical to the Pin Driver output waveform. This cannot be achieved because it is impossible to place each Pin Driver output pin right at each of the corresponding DUT input pins. The best one can expect is to get a channel with a phase delay that is linearly proportional to frequency. This means that a transmission line connected between the Pin Driver and the DUT must have ideal characteristics such as lossless, perfectly matched to both source and load, and of uniform characteristic impedance. Unfortunately, this is hard to achieve, particularly for a high pin count IC test system.

When the DUT is driving a channel, compensation is not possible, but the channel model can be used to predict the DUT output waveform at the output pad. Each PEC receiver input impedance can be measured, using FDR, by driving it from a reference Pin Driver through an alternative dummy DUT package connected as a passthrough rather than a short circuit to ground.

8.2 TRANSMISSION PATHS MODELLED BY SIGNAL FLOW GRAPHS

Elements in transmission paths considered here have been introduced in chapter 3. The details of each element to be used in the transmission path model are presented in this section.

8.2.1 Directional Couplers

In a conventional test system, most of the elements in the transmission path can be represented by two-port networks. In our proposed test system, a directional coupler is employed in each channel, where it can be represented as a four-port network or as two three-port networks if a dual directional coupler is used. Circuit diagrams and port notation for both types of coupler and their associated signal flow graphs are shown in Figures 5.13 to 5.15 in chapter 5.

The scattering matrix for parallel-coupled transmission lines can be written as

$$S_{coupler} = \begin{bmatrix} \Gamma_1 & T & K & I \\ T & \Gamma_2 & I & K \\ K & I & \Gamma_3 & T \\ I & K & T & \Gamma_4 \end{bmatrix} \tag{8.3}$$

where $\Gamma_n, n = 1,\ldots,4$ is the reflection coefficient of port n measured with the other ports terminated by a set of normalizing impedances. Each port could be normalized to a different impedance, usually a positive real impedance (we use $50\,\Omega$). Complex normalizing impedances can be used to account for line losses and dispersion. In practice, one measures S-parameters normalized to a real positive impedance. Transformation to another set of normalizing impedances can be done using the matrix renormalization methods described in chapter 4.

To determine crosstalk effects, one can model two adjacent channels using signal flow graphs similar to those shown in Figures 5.13 and 5.14. SAINATI and MORAVEC [1989] have reported a technique to predict crosstalk using a frequency domain approach. This technique is similar to ours except that here a scattering matrix and signal flow graph are used to represent crosstalk transfer functions.

Directional couplers used as sampling devices, are constructed using a TEM mode transmission line configuration such as coaxial cable or strip transmission line. When the coupled lines are surrounded by a homogeneous and isotropic medium, they can be analyzed using TEM even and odd modes of propagation. This will give approximate results for quasi-TEM coupled transmission lines such as microstrip, and ideally there is no forward crosstalk for a stripline case. However, a practical coupler has finite directivity that must be taken into account.

8.2.2 Circuit for Transmission Path Model

To compare results obtained from the SFG model with a SPICE simulation, a channel with a lossless uniform transmission line is considered. A directional coupler model is not included because SPICE (version 2G.6) lacks it. Scattering parameters of SFG analyses were obtained by direct circuit analysis, but in practice one would measure them using an Automatic Network Analyzer. The normalizing impedance is $Z_0 = 1/Y_0 = 50\Omega$.

Figure 8.5 shows the SPICE simulation model and its corresponding signal flow graph, representing a typical transmission path.

8.2.3 The Pin Driver

The Pin Driver is modelled by a signal source $e_{in}(t)$ in SPICE, and by $E_G(s)$ in the flow graph, where

$$E_G(s) = \frac{E_{in}(s)(1-\Gamma_G)}{2} \tag{8.4}$$

$E_{in}(s)$ = Laplace transform of $e_{in}(t) = \mathcal{L}[e_{in}(t)]$, and

$$\Gamma_G = \frac{R_G - Z_0}{R_G + Z_0}$$

For $R_G = Z_0$, the amplitude of the SFG signal source, $E_G(s)$, is half of the SPICE signal source, $E_{in}(s)$, because E_G is defined as the voltage which appears across the

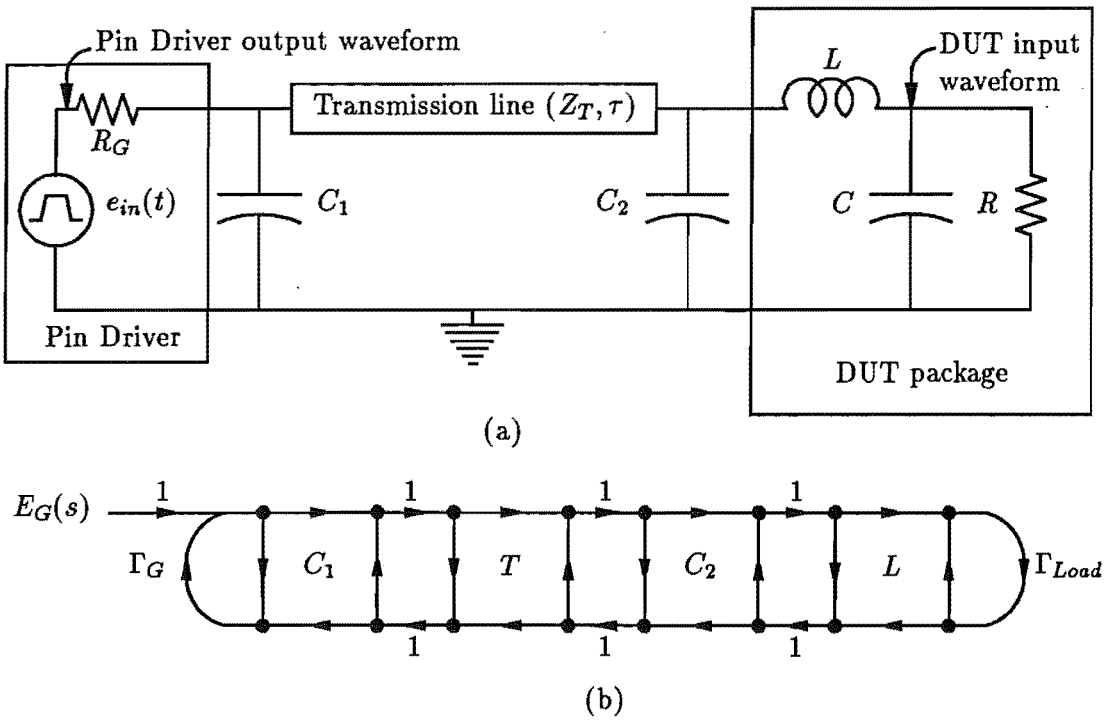


Figure 8.5 (a) Circuit model for SPICE simulation (b) signal flow graph representation.

output terminals when the source is terminated with a matched load, whereas E_{in} is defined as the voltage which appears across the output terminals when the source is terminated with an open circuit (*i.e.* Thevenin equivalent source).

8.2.4 The Transmission Line

The scattering matrix for a lossless uniform transmission line, with propagation delay τ and characteristic impedance Z_T, is

$$S_T = \frac{1}{1-\rho_T^2 e^{-2s\tau}} \begin{bmatrix} -\rho_T(1-e^{-2s\tau}) & e^{-s\tau}(1+\rho_T^2(e^{-2s\tau}-1)) \\ e^{-s\tau}(1+\rho_T^2(e^{-2s\tau}-1)) & -\rho_T(1-e^{-2s\tau}) \end{bmatrix} \tag{8.5}$$

where

$$\rho_T = \frac{Z_0 - Z_T}{Z_0 + Z_T}$$

Equation 8.5 was derived using scattering matrix renormalization, described in section 4.3 in chapter 4.

8.2.5 The DUT Model

The DUT input impedance is modelled by a parallel resistor and capacitor in SPICE, and by Γ_{Load} in the flow graph, where

$$\Gamma_{Load} = \frac{Y_0R - (1 + sCR)}{Y_0R + (1 + sCR)} \tag{8.6}$$

This model is not specific to any particular DUT, being an example of a linear approximation to a DUT input structure together with its parasitics. In practice, a test engineer will select an appropriate DUT model to be used in the optimization process.

Note that this DUT model is different from the load model used in the previous chapters. The DUT model, used in chapter 7 to fit the measured reflection coefficients, includes a package parasitic (appears as inductor in Figure 8.5). To determine the waveform at the DUT input, the inductor is separated from the DUT model and is included to the transmission path model as a discontinuty which will be described next.

8.2.6 The Discontinuity Models

C_1, C_2 and L, represent simple discontinuity models. Scattering matrices for a shunt capacitor and a series inductor are:
For a shunt capacitor (C),

$$S_C = \frac{1}{sC + 2Y_0} \begin{bmatrix} -sC & 2Y_0 \\ 2Y_0 & -sC \end{bmatrix} \tag{8.7}$$

and for a series inductor (L)

$$S_L = \frac{1}{sL + 2Z_0} \begin{bmatrix} sL & 2Z_0 \\ 2Z_0 & sL \end{bmatrix} \tag{8.8}$$

More complex discontinuity models such as those in Figure 8.6 can be used.

The scattering parameters of these complex discontinuty models can be obtained directly by analysis, or by partitioning them into cascaded graphs of simple single element models and then solving for the overall characteristics. Their scattering matrices are:
For the RL circuit (Figure 8.6 (a)),

$$S_{RL} = \frac{1}{R + sL + 2Z_0} \begin{bmatrix} R + sL & 2Z_0 \\ 2Z_0 & R + sL \end{bmatrix} \tag{8.9}$$

For the GC circuit (Figure 8.6 (b)),

$$S_{GC} = \frac{1}{G + sC + 2Y_0} \begin{bmatrix} -(G + sC) & 2Y_0 \\ 2Y_0 & -(G + sC) \end{bmatrix} \tag{8.10}$$

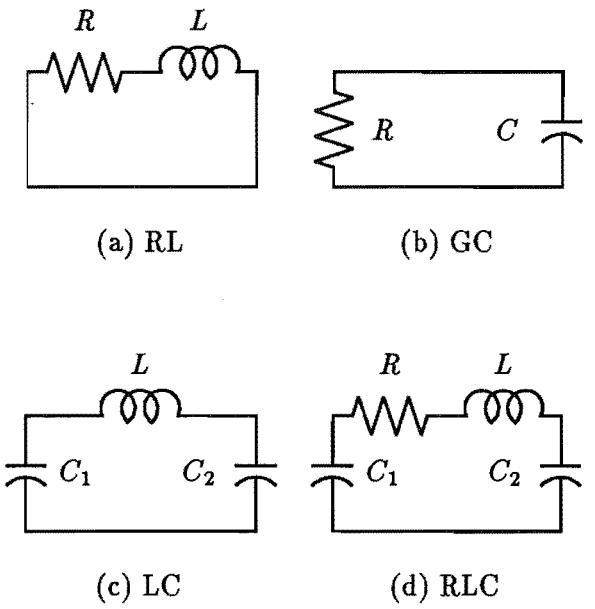


Figure 8.6 Some discontinuity models.

For the LC circuit (Figure 8.6 (c)),

$$S_{LC} = \frac{1}{A_1 + A_2 + 2/Z_0} \begin{bmatrix} A_2 - A_1 & 2/Z_0 \\ 2/Z_0 & A_2 - A_1 \end{bmatrix} \tag{8.11}$$

where

$$A_1 = LC_1C_2s^3 + \frac{LC_1s^2}{Z_0} + (C_1 + C_2)s$$

$$A_2 = \frac{LC_2s^2}{Z_0} + \frac{Ls}{Z_0^2}$$

For the RLC circuit (Figure 8.6 (d)),

$$S_{RLC} = \frac{1}{A_3 + A_4 + 2/Z_0} \begin{bmatrix} A_4 - A_3 & 2/Z_0 \\ 2/Z_0 & A_4 - A_3 \end{bmatrix} \tag{8.12}$$

where

$$A_3 = A_1 + RC_1C_2s^2 + \frac{RC_1s}{Z_0}$$

$$A_4 = A_2 + \frac{RC_2s}{Z_0} + \frac{R}{Z_0^2}$$

8.3 THE PROPOSED COMPENSATION METHOD

To compute a compensation waveform, the channel and load characteristics must be determined. The load model obtained from the procedures described in chapter 7 can

be use to simulate its frequency characteristic. This section describes the method used to achieve the compensation waveforms for the two example cases presented in this thesis.

8.3.1 The Input

The input waveform is obtained from SPICE transient analysis of a linear voltage controlled voltage source, as shown in Figure 8.7, simulating an ideal signal source driving a low-pass filter (LPF). The characteristic of the low-pass filter is adjusted until the required waveform is achieved.

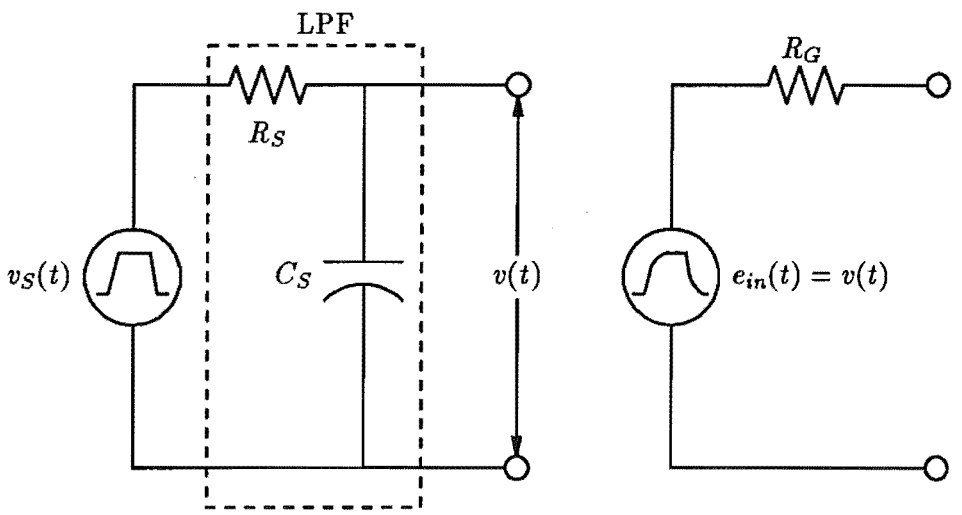


Figure 8.7 Circuit diagram to generate an input waveform.

Figure 8.8 shows an example of an exponentially rising signal with a 10%–90% rise time of 1 ns, 50% pulse width of 10 ns, and repetition rate of 50 MHz. Amplitude and phase spectra of the input signal are shown in Figure 8.9 (a) and (b) respectively.

8.3.2 Computing of Fourier Components

Complex Fourier coefficients were computed using Discrete Fourier Transform (DFT) rather than the Laplace transform because both measurement and numerical computation are performed in the steady state. The sampling period was chosen to preserve the time domain resolution. The number of samples ($N = 1000$) is determined by the need to calculate the discrete spectrum at each harmonic of the input waveform (at 50 MHz intervals). This spreads the computation bandwidth to 50 GHz, but in practice the meaningful bandwidth is only up to 1–2 GHz. Equations to implement the transform–inverse transform are [LITTLE and SHURE, 1988]

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{kn} \tag{8.13}$$

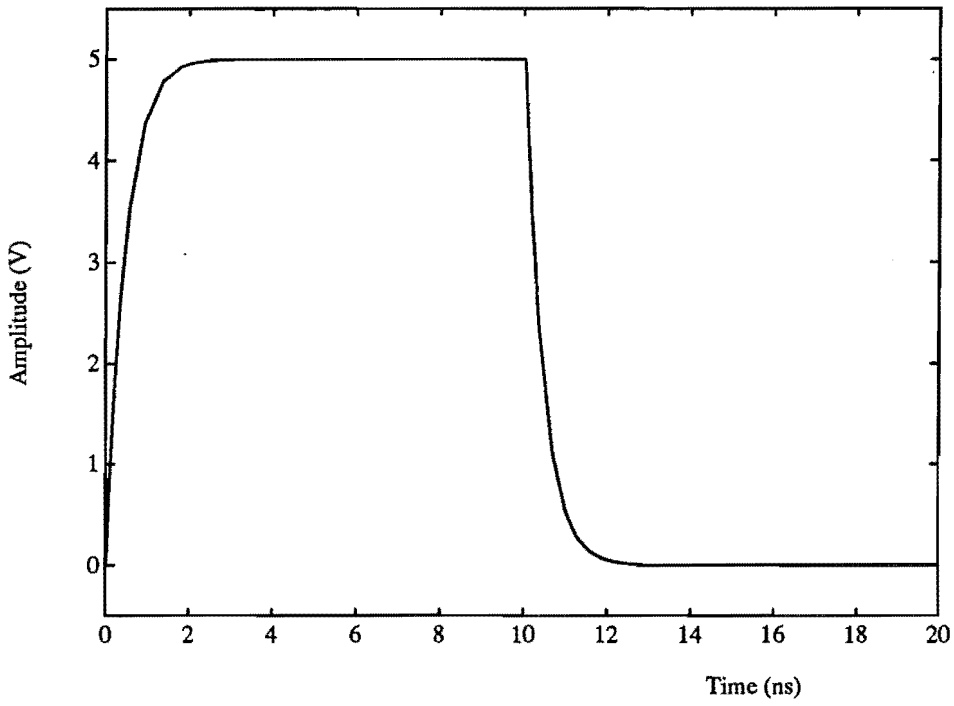


Figure 8.8 An example of input waveform.

$$x(n) = \frac{1}{N}\sum_{k=0}^{N-1} X(k)W_N^{-kn} \tag{8.14}$$

where $W_N^{\pm kn} = e^{\pm j(2kn\pi/N)}$ and N is the number of sample points.

Fourier series technique using a trapezoidal waveform as an input signal has been used by SAINATI and MORAVEC [1989]. Any input waveform could be used, provided it can be represented by a Fourier series, since the impulse response of the channel is known.

8.3.3 The Compensation Waveform

A compensation waveform can be derived either from the differences between a required waveform and the waveform at the output of the linear system, or the differences between the spectrum of both signals. Both methods yield the same results. The required waveform is, in this case, an input waveform delayed by the transmission path propagation delay τ.

The compensation waveform required at the Pin Driver output, obtained from the input spectrum and the channel transfer function, is

$$E_{com}(s) = \frac{\left[e^{-j\omega\tau} - H(s)\right] E_G(s)}{H(s)}. \tag{8.15}$$

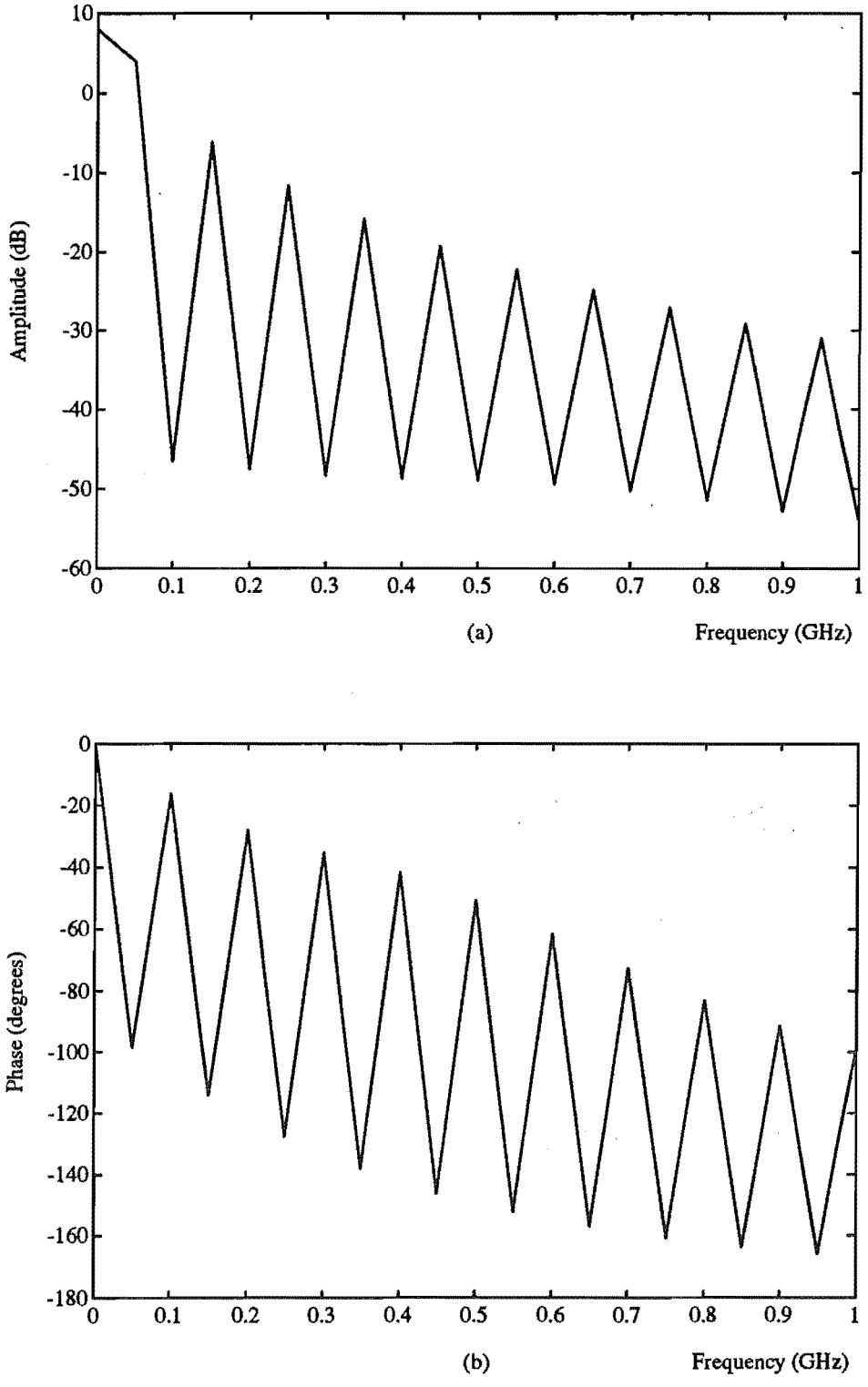


Figure 8.9 An example of input spectrum from *d.c.* to 1 GHz (a) magnitude (b) phase.

In the case of nonlinear termination, a compensation waveform should be obtained in the time domain because nonlinear effect must be simulated in time domain. The compensation waveform may then be transformed into the frequency domain, and then the compensation waveform required at the Pin Driver output can be computed in similar manner using equation 8.15, but in this case the load is not included in $H(s)$. All processes could be performed in the time domain using convolution and deconvolution techniques, but multiplication and division in the frequency domain is considerably simpler to implement.

8.3.4 Determination of the Overall Transfer Function

The overall channel frequency characteristics may be found by signal flow graph reduction described in section 4.4 of chapter 4, or by representing each two-port element by a transfer scattering matrix, (or T-parameter matrix) [GUPTA *et al.*, 1981]. The T-parameter representation is defined as [CARLIN and GIORDANO, 1964]

$$\begin{aligned} b_1 &= T_{11}b_2 + T_{12}a_2 \\ a_1 &= T_{21}b_2 + T_{22}a_2 \end{aligned} \tag{8.16}$$

The overall response may be computed by the chain product of all T-matrices which is then converted back to S-parameters. The T-matrix method, illustrated in Figure 8.10, was used to obtain the overall frequency characteristics of the two example channels.

$S \Leftrightarrow T$ transformations are,

$$T = \frac{1}{S_{21}} \begin{bmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{bmatrix} \tag{8.17}$$

and

$$S = \frac{1}{T_{22}} \begin{bmatrix} T_{12} & T_{11}T_{22} - T_{12}T_{21} \\ 1 & -T_{21} \end{bmatrix} \tag{8.18}$$

The MAPLE procedures which implement a symbolic form of the above two equations are given in appendix F.

8.3.5 Finding the DUT Input Waveform

To find the waveform at the DUT input (Figure 8.5 (a)) one further reduces the graph, using a topological graph reduction method described in section 4.4 of chapter 4, to yield the results shown in Figure 8.11 (a). The incident wave $a = \widehat{S}_{21}E_G$ where

$$\widehat{S}_{21} = \frac{S_{21}}{1 - \Gamma_{Load}S_{22}} \tag{8.19}$$

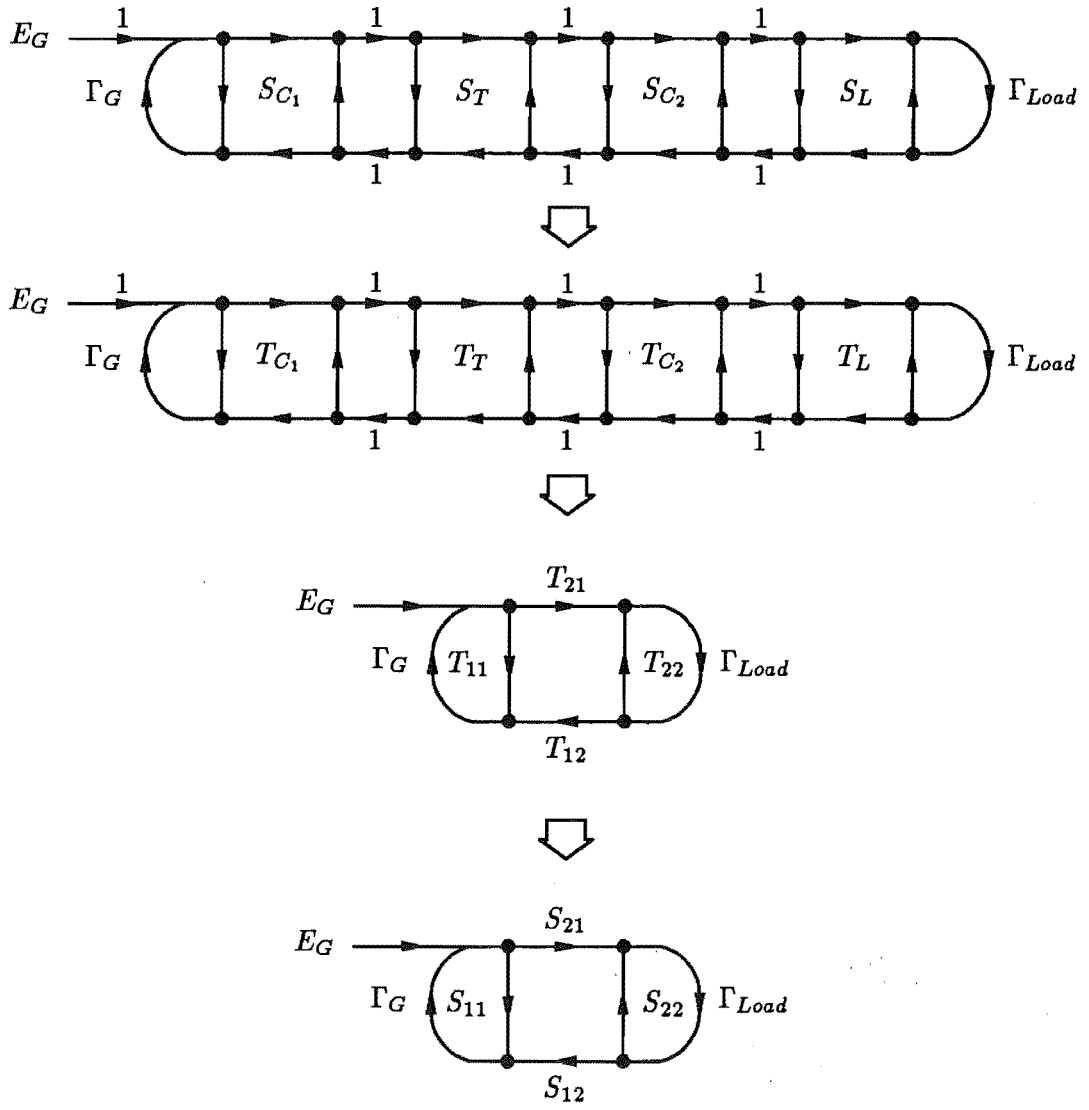


Figure 8.10 Transfer scattering matrix method to achieve the overall channel characteristics.

and the reflected wave $b = a\Gamma_{Load} = \widehat{S}_{21}E_G\Gamma_{Load}$. The DUT input waveform is obtained from the inverse Laplace transform of the sum of the incident and reflected waves, $\mathcal{L}^{-1}[a+b] = \mathcal{L}^{-1}[(1+\Gamma_{Load})\widehat{S}_{21}E_G]$.

This flow graph can be thought of as a linear system with a transfer function $H(s) = (1+\Gamma_{Load})\widehat{S}_{21}$ illustrated in Figure 8.11 (b).

$H(s)$ can be formed as a function of the circuit elements in the channel. A general equation, which contains many terms due to multiple reflections in the channel, is presented in appendix H. Here, two examples of the magnitude and phase responses

for matched and mismatched channels are presented.

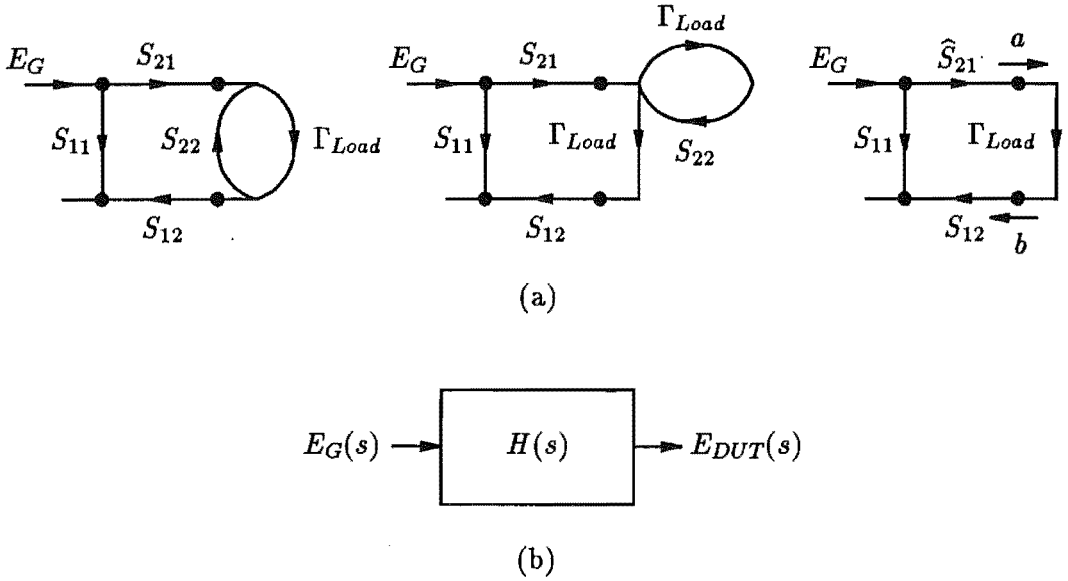


Figure 8.11 (a) Signal flow graph representation of the example channel simplified by a signal flow graph reduction method. (b) a corresponding linear system.

8.4 COMPENSATION WAVEFORMS FOR THE EXAMPLE CASES

The channel transfer function for each case was obtained by substituting corresponding values, listed in Table 8.1, into the general channel equation. These values were selected to demonstrate the capability of the proposed technique to correct for timing error and waveform distortion. The characteristic impedance in the mismatched line case results in a reflection coefficient magnitude of 0.2, which is quite severe but within reason. Frequently, one may encounter not only mismatched but also nonuniform and lossy transmission lines. Provided the non-uniformity and loss are not extreme, the method outlined in this chapter should still be effective. The equipment manufacturer and test engineer will be able to minimize such deficiencies.

	R_G (Ω)	Z_T (Ω)	τ (ns)	C_1 (pF)	C_2 (pF)	R (Ω)	L (nH)	C (pF)
matched line	50	50	2	5	5	1K	5	10
mismatched line	50	75	2	5	5	1K	5	10

Table 8.1 Parameter values for matched and mismatched channels.

The two transfer functions have the same form, which is

$$H(s) = \frac{H_N(s)}{H_{D1}(s) + H_{D2}(s) + H_{D3}(s) + H_{D4}(s) + H_{D5}(s)} \tag{8.20}$$

8.4.1 The Matched Channel

For the matched channel case,

$$\begin{aligned}
H_N(s) &= 0.04(21 + 10^{-8}s)e^{(-2\times10^{-9}s)} \\
H_{D1}(s) &= (-1.25 \times 10^{-39}e^{(-4\times10^{-9}s)} + 1.25 \times 10^{-39})s^4 \\
H_{D2}(s) &= (4.875 \times 10^{-30}e^{(-4\times10^{-9}s)} + 1.5125 \times 10^{-29})s^3 \\
H_{D3}(s) &= (-7.45 \times 10^{-20}e^{(-4\times10^{-9}s)} + 1.165 \times 10^{-19})s^2 \\
H_{D4}(s) &= (9.5 \times 10^{-11}e^{(-4\times10^{-9}s)} + 7.09 \times 10^{-10})s \\
H_{D5} &= 0.84
\end{aligned}$$

To illustrate the characteristics of the matched transmission path, the magnitude and phase response of the transfer function is plotted over the frequency range from *d.c.* to 1 GHz in Figure 8.12. In the actual computation, the transfer function is repetitive at $\pm 1/\mathrm{T} = \pm 50\,\mathrm{GHz}$ (T = time domain sampling period = 20 ps).

8.4.2 The Mismatched Channel

For the mismatched channel case,

$$\begin{aligned}
H_N(s) &= 0.0384(21 + 10^{-8}s)e^{(-2\times10^{-9}s)} \\
H_{D1}(s) &= (-1.8 \times 10^{-39}e^{(-4\times10^{-9}s)} + 1.8 \times 10^{-39})s^4 \\
H_{D2}(s) &= (2.22 \times 10^{-30}e^{(-4\times10^{-9}s)} + 1.698 \times 10^{-29})s^3 \\
H_{D3}(s) &= (-1.0136 \times 10^{-19}e^{(-4\times10^{-9}s)} + 1.4168 \times 10^{-19})s^2 \\
H_{D4}(s) &= (-5.456 \times 10^{-11}e^{(-4\times10^{-9}s)} + 8.264 \times 10^{-10})s \\
H_{D5}(s) &= 0.688 + 0.1184e^{(-4\times10^{-9}s)}
\end{aligned}$$

The characteristics of the mismatched transmission path are plotted over the same frequency range, as shown in Figure 8.13.

8.4.3 Verification of The Model

The channel transfer functions obtained from the SFG method were verified by comparing the DUT waveforms computed from that transfer function with the results from a SPICE simulation. The SFG method gives identical results to the SPICE AC steady-state analysis but differs slightly from the SPICE transient analysis, as depicted in Figure 8.14.

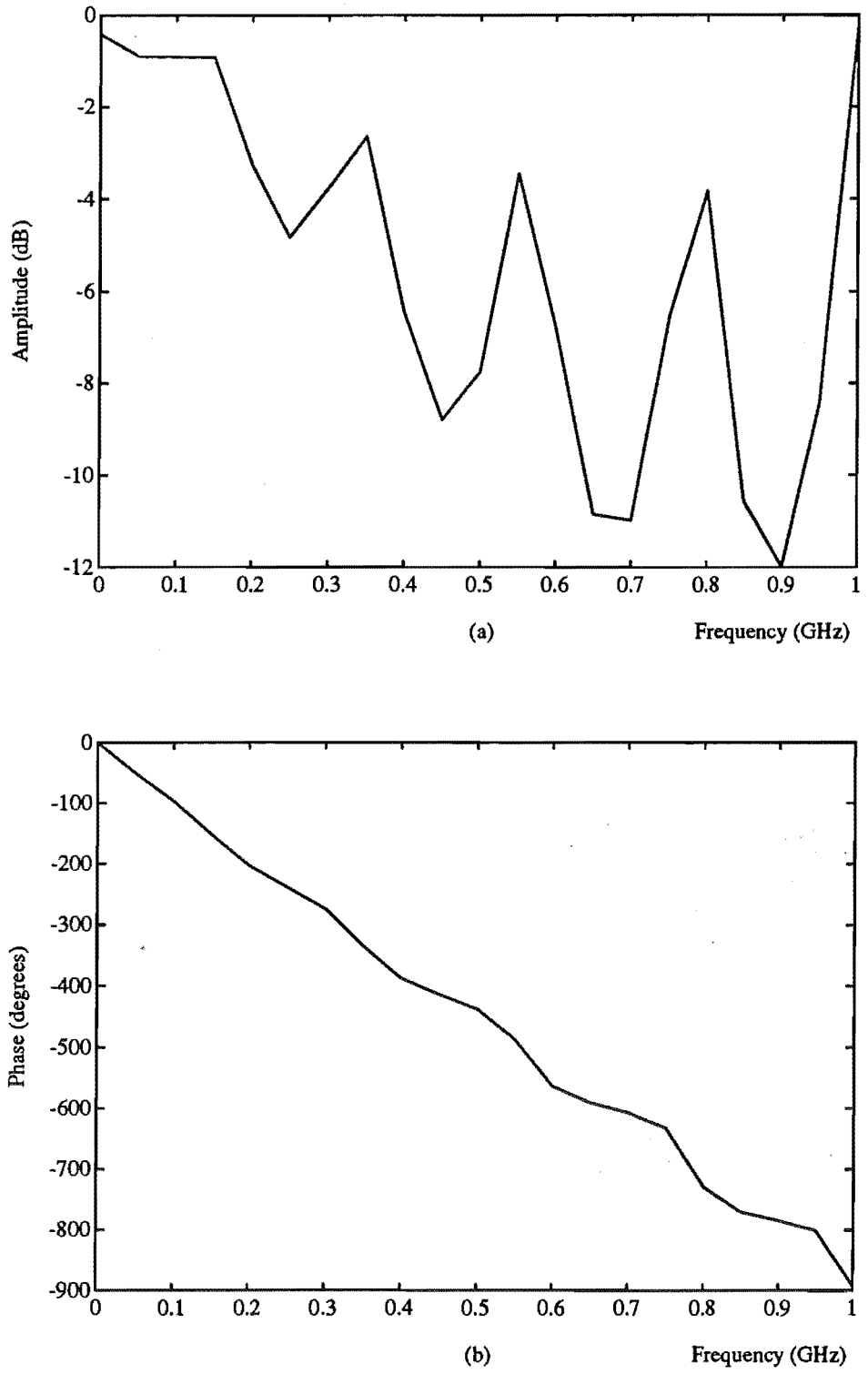


Figure 8.12 (a) Magnitude response of the matched channel (b) phase response of the matched channel.

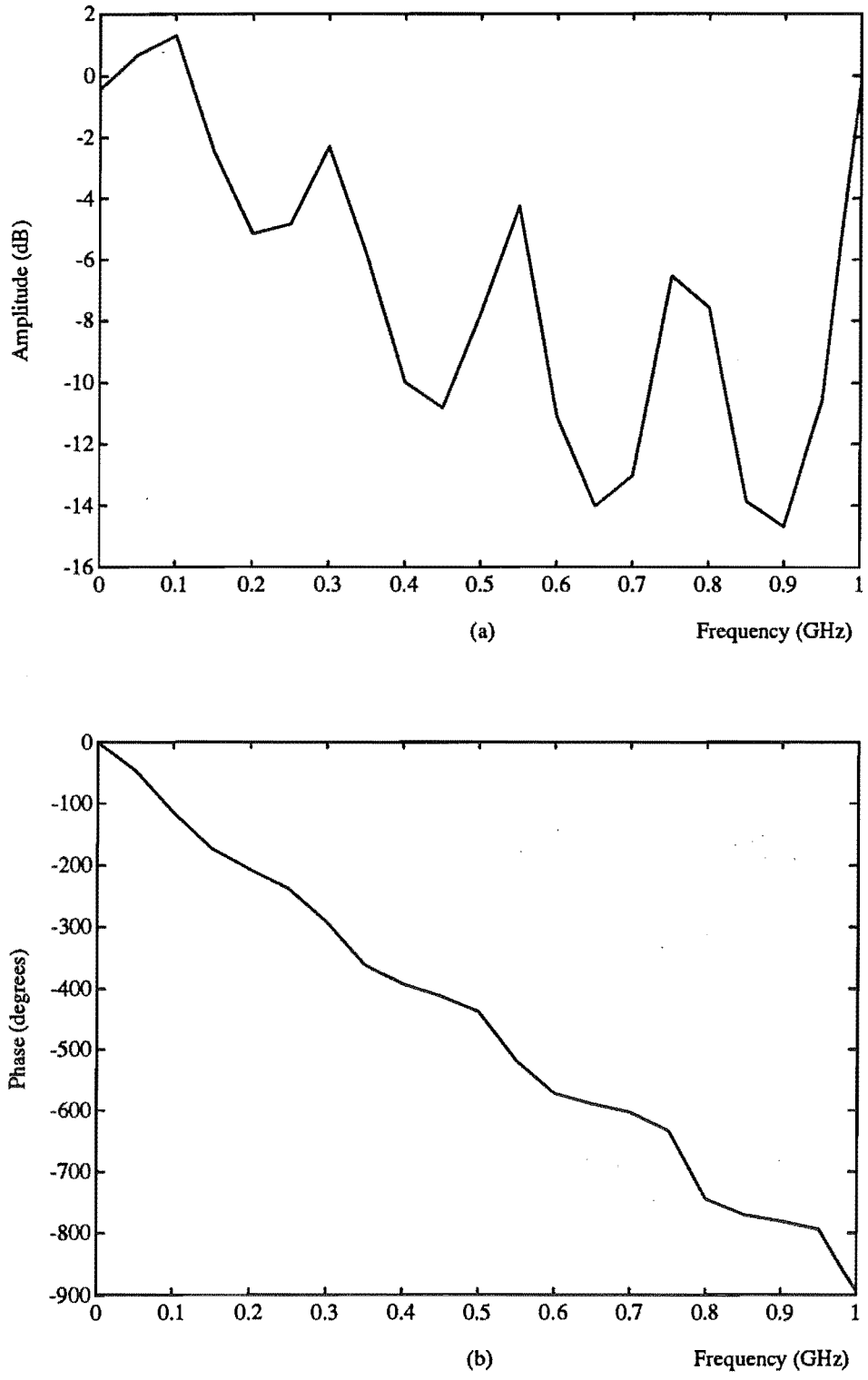


Figure 8.13 (a) Magnitude response of the mismatched channel (b) phase response of the mismatched channel.

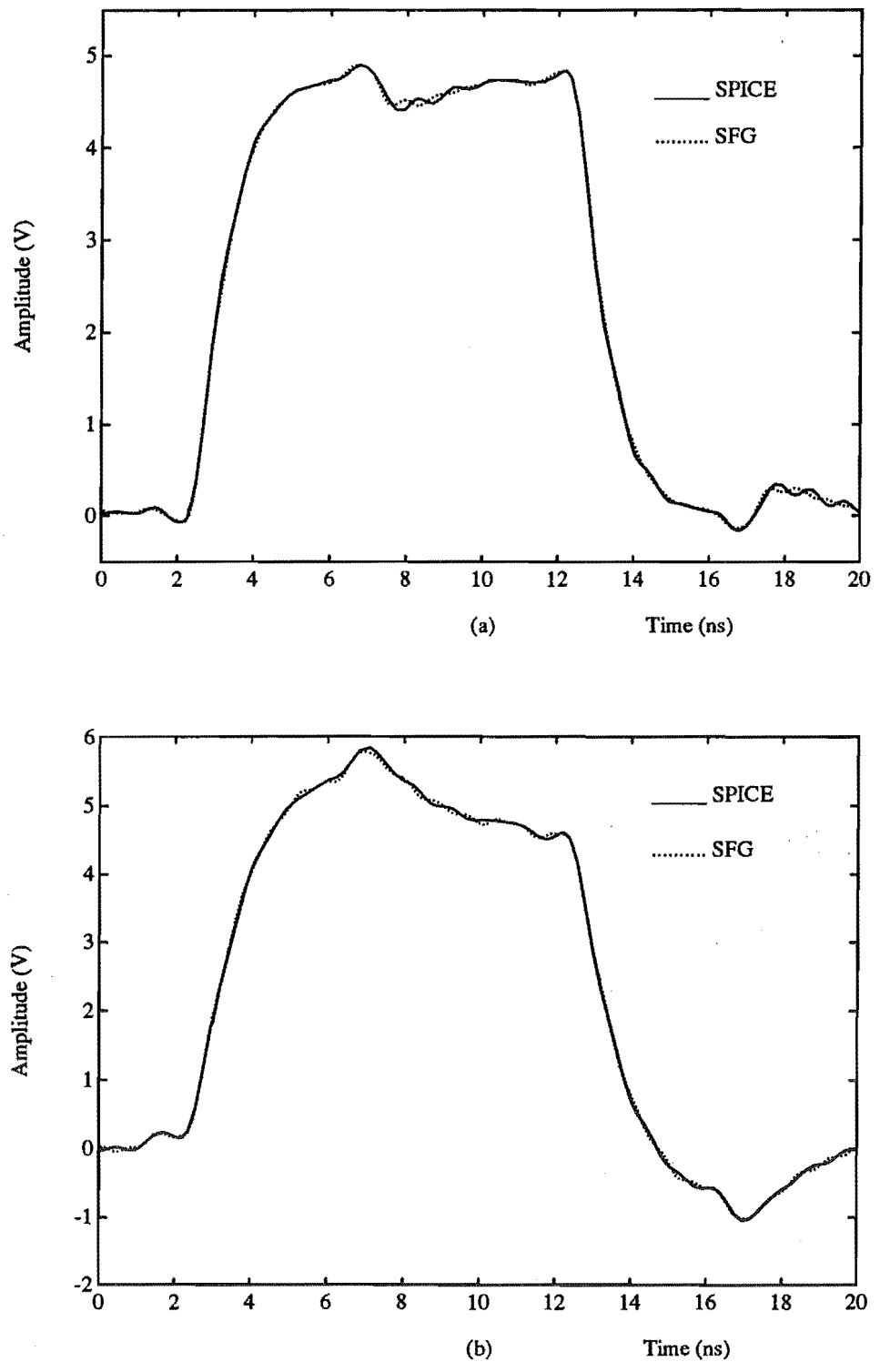


Figure 8.14 Comparison of DUT waveforms from SFG method and SPICE transient analysis (a) matched channel (b) mismatched channel.

The differences arise because the SFG method has been developed for the steady state and the harmonics were summed in a finite bandwidth (25 GHz). If the computation bandwidth is increased we will get a closer result, but because the higher harmonics of the input signal spectrum are well below the expected channel noise level, the chosen computation bandwidth is adequate. A negligibly small accumulated roundoff error occurs during computation of the Fourier coefficients.

8.4.4 Computed Compensation Waveform

The compensation waveforms were computed from *d.c.* and the first 25 harmonics of the spectrum of $E_{com}(s)$. Compensation waveforms generated by hardware need include no higher harmonic than the 25^{th} because the remainder contain negligible energy, comparable to the noise level. Practical compensation waveforms will differ somewhat from simulated waveforms because of hardware complexity limitations imposed by size and cost constraints. Implementation methods will depend upon acceptable DUT waveform tolerances.

Figure 8.15 illustrates various compensation waveforms computed from only the fundametal component, 5, 10 and 25 harmonics. When the number of harmonics is higher than 15, the compensation waveforms are very similar.

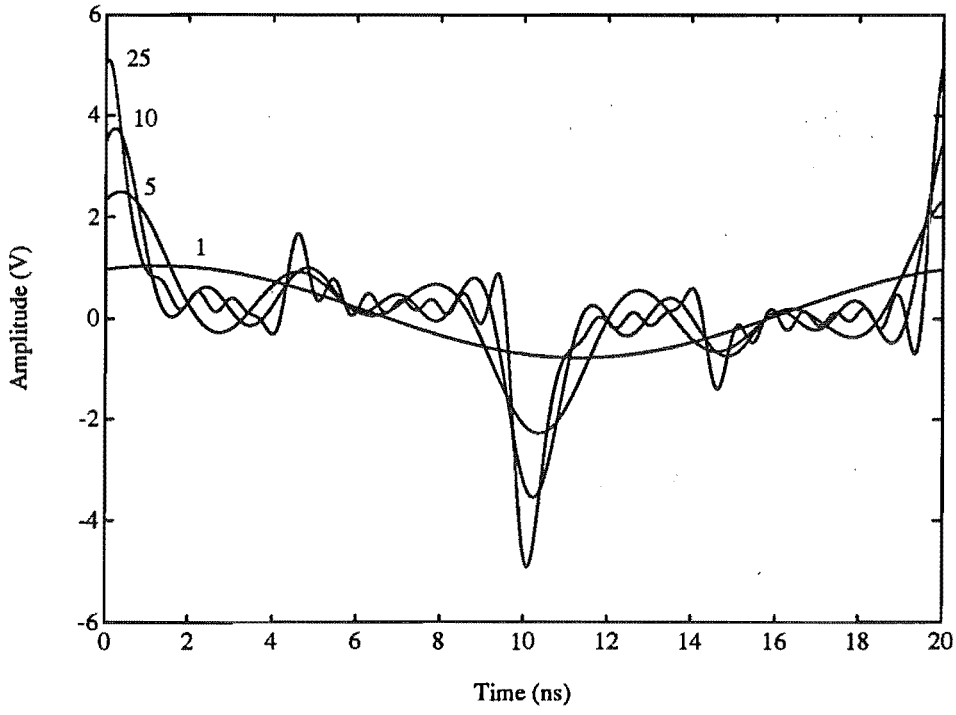


Figure 8.15 Computed compensation waveforms from different numbers of harmonics, for the matched channel.

8.4.5 Approximated Compensation Waveform

Each of the approximate compensation waveforms was synthesized by combining three separate operations. The first compensates for reflections from S_{11} of each element in the channel and Γ_{Load}, and the second cancels out reflections from S_{22} and Γ_G. These waveforms can be produced by approximate differentiation of a fast transition by single-time-constant (STC) networks. The third restores the pulse amplitude at the DUT to the required value by increasing the Pin Driver output amplitude by $1/H(d.c.)$.

The first two components of the computed compensation are approximated by a waveform generated by passing a fast transition signal through STC networks. The computed compensation in this case does not include the *d.c.* component since that will be compensated for by increasing the PEC output amplitude.

Figure 8.16 illustrates the processes to obtain the approximated compensation waveforms for the example channels. The output from the STC circuits is compared against the computed waveform, using a least squares objective function. The simplex algorithm is employed in the minimization procedure.

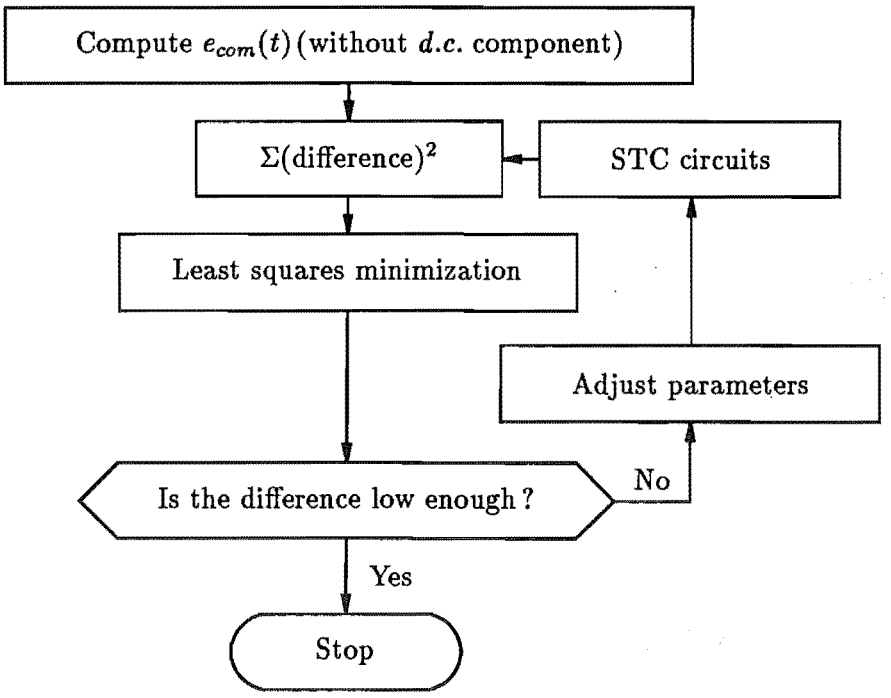


Figure 8.16 Processes to achieve an approximated compensation waveform.

The SPICE circuit used for these two examples includes low-pass filters to control rise and fall times, as shown in Figure 8.17. This elementary demonstration, would translate into more complex hardware, able to independently control the 8 rise and fall times and amplitudes of the approximate compensation waveforms.

The values of resistor and capacitor were achieved by minimizing the least squares

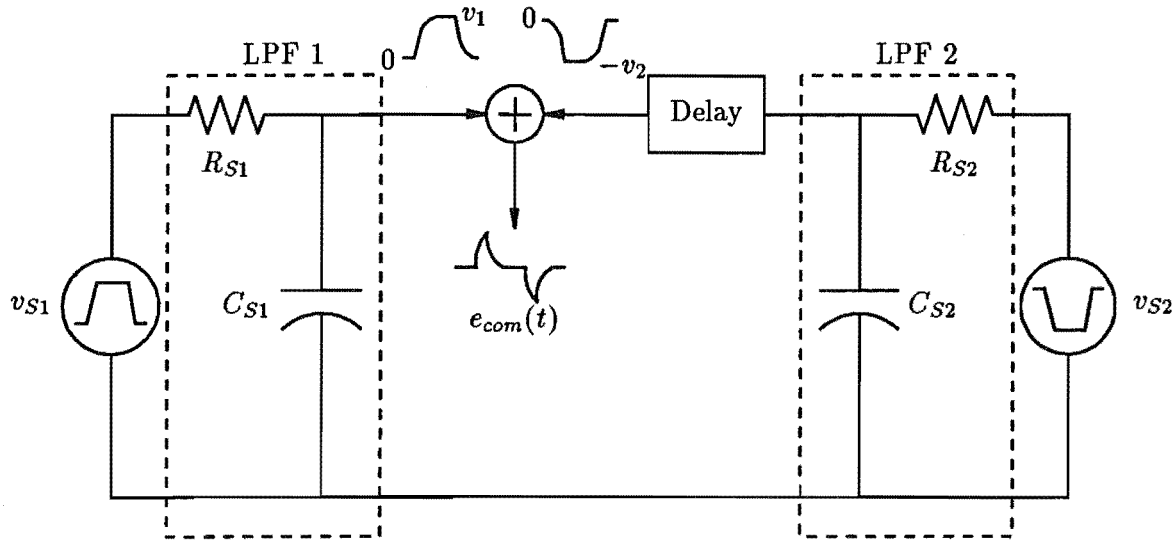


Figure 8.17 Circuit diagram for STC circuits used to generate the approximated compensation waveforms.

error between the waveform generated by the circuit and that computed from the SFG model. In the minimization procedure, the amplitude and time constant of the output from the STC circuit were adjusted to give minimum error. Figure 8.18 shows compensation waveforms, both computed and approximate hardware-generated, to be added to the Pin Driver. The input waveform is delayed by 2.72 ns to illustrate the relative timing between the compensation and the basic Pin Driver output waveforms.

Very good compensations were achieved for edge-placement timing because the required shapes are similar to those generated by simple RC networks. This first attempt employs only a single RC circuit, and a more complex circuit might give even better results. In general, the compensation waveform can be adjusted to satisfy any particular requirement such as correct timing at 2.5 V but this is achieved through sacrificing some less critical parameters, for example, overshoot or undershoot of the waveform.

8.5 SIMULATION RESULTS

The author synthesized the computed compensation waveforms in SPICE by defining a piece-wise linear source, using 100 sample points (every 0.2 ns). The SPICE simulated hardware-generated waveforms were synthesized by methods similar to those used to create the main Pin Driver output waveform. The SPICE input files appear in appendix G.

Figures 8.19 (a) and (b) compare SPICE simulation results for matched and mismatched lines. The computed waveforms (dashed lines) refer to those compensated

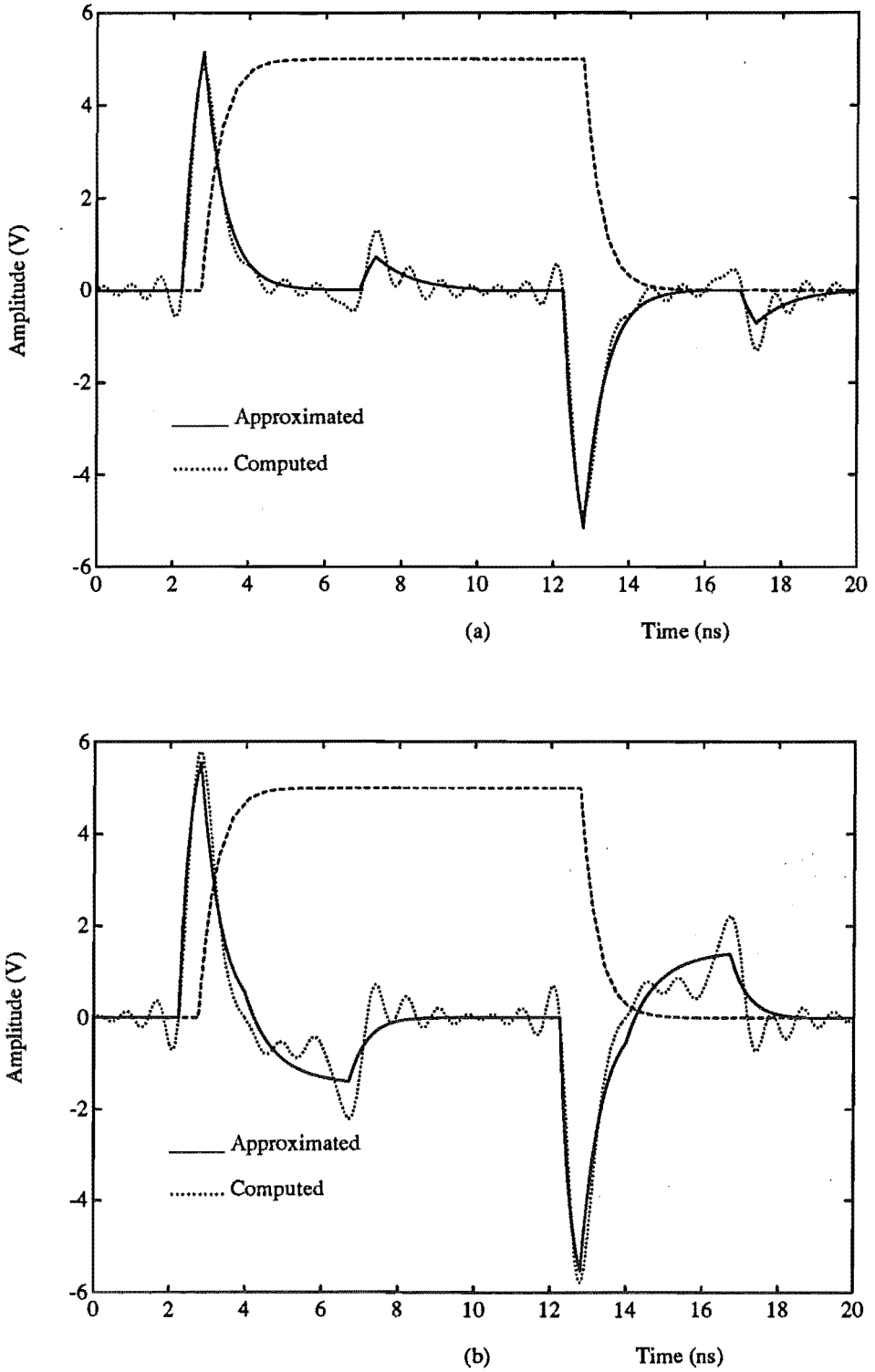


Figure 8.18 Compensation waveforms, computed and hardware-generated, required at the Pin Driver output, shown in relation to the basic output (a) matched channel (b) mismatched channel.

using waveforms synthesized by a piece-wise linear source whereas the approximated waveforms (dotted lines) refer to those compensated by waveforms obtained through STC networks.

Both the computed and hardware-generated compensation waveforms almost completely correct edge-placement timing errors ($\approx$ 900ps) for both matched and mismatched cases. The computed compensation has reduced reflection effects to an acceptable level (less than $\pm$ 100mV). In the hardware-generated case, less improvement is evident, but this may not be serious because the residual reflection is small and is well within the typical noise margin.

8.6 A REALISTIC IMPROVEMENT

It is rather premature to discuss a realistic improvement to be gained from this effort since major hardware components have not yet been built. Simulation results reveal the potential benefit and they represent some typical cases only. A transient simulator that can simulate lossy multiconductor transmission lines with nonlinear terminations should provide closer results to reality.

The actual improvement depends not only on the technical factors but also on the economic considerations. Design effort can be put to optimize the improvement but at what cost and who is ready to pay for such extra cost.

The main contribution to the uncertainty in achieving the correct timing can be divided into three groups.

1. Error in channel characteristic determination which is proportional to the number of elements in the channel and the inaccuracy of the equipment used to characterize them.

2. Error in load characteristic determination which depends on the number of elements in the load model, the accuracy of the detector circuit in the FDR system, and how closely they represent the actual load.

3. Error in approximating the compensation waveform which is inversly proportional to hardware complexity and cost.

There is inter-relation between these error sources: for example, the inaccurate characterization of the channel would affect the FDR measurement and therefore the load model determination and compensation waveform.

Waveform "quality" is even more difficult to quantitatively assess since the criteria of a "good" waveform will vary from case to case. However, one certain advantage from this technique should be that test engineers will be *better* able to control critical waveform parameters.

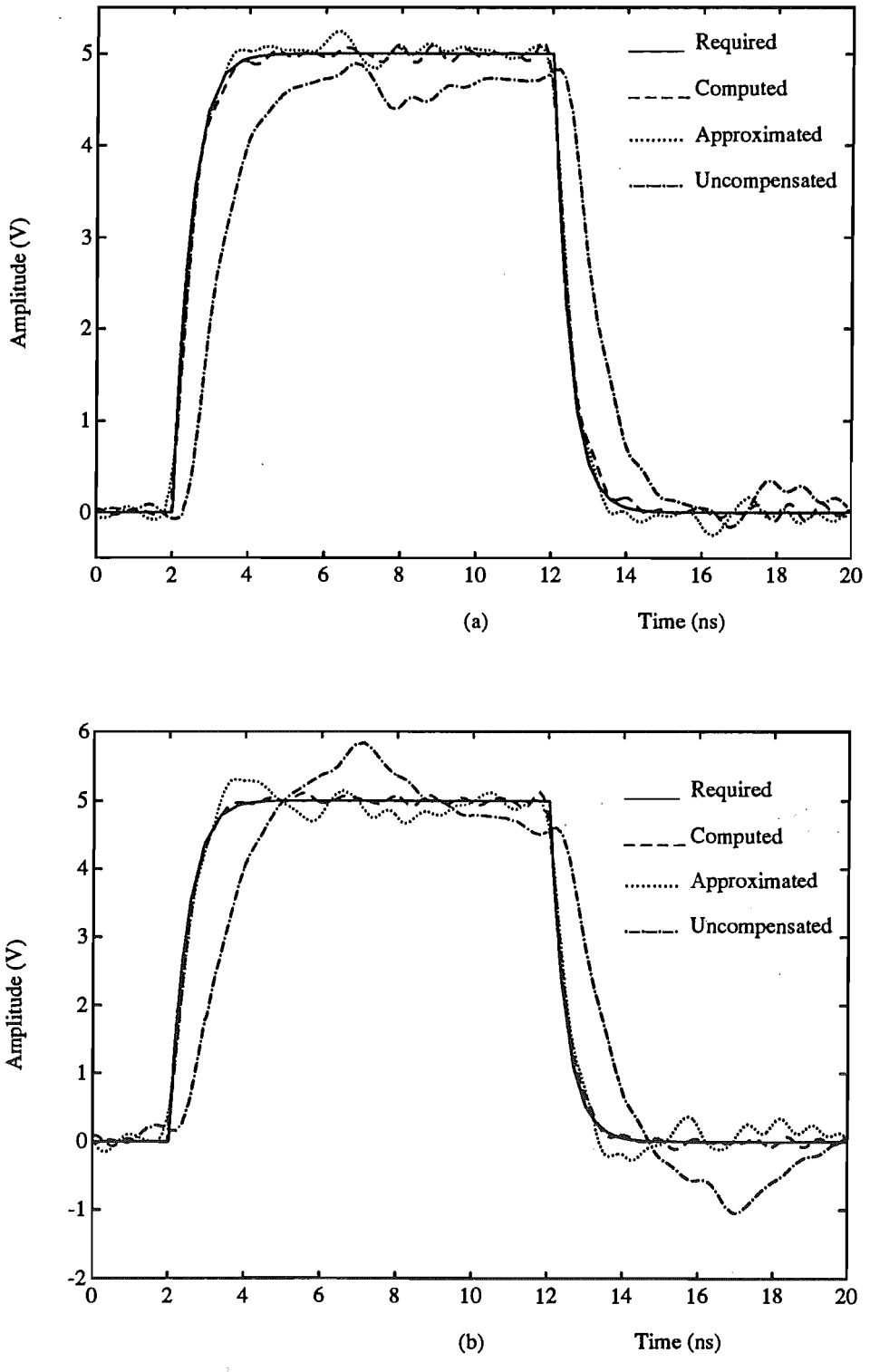


Figure 8.19 SPICE simulation results (a) matched channel(b) mismatched channel.

8.7 CONCLUSION

The transmission path between a PEC and DUT in a high speed, high performance, test and verification system can be modelled using a signal flow graph technique. The channel transfer functions obtained from the SFG method give results identical to the SPICE AC steady state analysis, but differ slightly from the SPICE transient analysis.

Simulation results show that compensation waveforms computed from the channel characteristic almost completely correct edge-placement timing errors and greatly reduce reflection effects. Implementation of compensation waveforms by simple hardware is possible, leading to edge-placement correction which is almost as good as that obtained from a theoretically computed compensation waveform.

Such improvement of edge-placement accuracy and waveform quality should usefully improve the confidence level of results from such a test system. A consequent benefit would be a reduction in the required guardband, allowing characterization of the DUT closer to its true performance, and fewer test rejects.

CHAPTER 9

CONCLUSION AND RECOMMENDATIONS

This chapter summarises my thesis and suggests direction for further development.

9.1 SUMMARY

The proposed calibration method, described in chapter 3, requires the following additional hardware:

1. A directional coupler and detector circuit.
2. A compensation waveform generator.
3. A unity gain buffer and PIN diode switches.

This thesis has investigated the first two items, and the results are presented in chapters 5 to 8. To summarise the propose procedure, we present a sequence of calibration steps:

- Perform timing alignment at the Pin Driver output using a detector circuit outlined in section 5.1.4.6. This procedure corrects for timing errors that occur within the PEC. Subsequent procedures will account for timing errors caused by an imperfect channel, including the DUT package.
- Perform FDR measurements at n discrete frequencies. The number of measurements (n) depends on the DUT model complexity and the operating clock frequency.
- An optimization program is required at this stage to find a DUT model that has frequency characteristics close to the previously measured values.
- Once the complete channel model is known, a compensation waveform can be computed. Approximation to this computed compensation waveform is generally required, due to hardware limitations.

9.2 CONCLUSION

I have presented a means of improving the edge-placement accuracy and waveform quality in high performance ASIC testers. The study shows that the proposed calibration method can be used to minimize timing skew, maintain signal integrity at the DUT, and actively reduce waveform errors caused by uncertain DUT loading and transmission path imperfections.

The following conclusions can be drawn:

1. **Frequency Domain Reflectometry**
   FDR can be employed to measure voltage reflection coefficients of both the load (DUT) and PEC receiver ends of the transmission path. A vector voltmeter has been used to measure the magnitude and phase of the incident and reflected waves in the FDR experiment. FDR measurement accuracy is within the measuring equipment specification for a matched dual directional coupler, and is good enough for first-order correction of transmission path imperfections and DUT loading. Time domain waveforms can be obtained using Discrete Fourier Transformation (DFT).

   Experimental results show that the SFG technique can be used to correct the measured values, yielding results comparable to those obtained from an automatic network analyzer (HP8510). However, this technique requires accurate knowledge of S-parameters for all elements in the measurement configuration.

2. **Thickfilm-Hybrid Directional Coupler**
   Two prototypes, single and dual directional couplers, have been designed and implemented using TFH. Both couplers have a strip transmission line form that supports a TEM propagation mode. The dual coupler is more suitable because it is easier to achieve good isolation between ports 3 and 4. The dual coupler's isolation factor depends only on the matching condition of internal resistors whereas the single coupler's depends on external terminations which are more difficult to control.

   The prototypes' reflection coefficients ($S_{ii}; i = 1, \ldots, 4$) have larger magnitude than those of the HP778D, principally because the TFH coupler characteristic impedance is higher than $50\,\Omega$, and partly because of the adaptors required to interface the prototype BNC connectors to the measurement equipment type-N connectors. The eventual implementation, which will include detector circuits on the same substrate, should exhibit better performance.

3. **Optimization Technique**
   Load models that represent the DUT input pin or PEC receiver are obtained through a direct search optimization algorithm. In this initial study, only linear time-invariant load models are considered. This thesis implements two direct

search methods, the pattern search and simplex algorithms. Results show that both methods work satisfactorily because the objective function is unimodal and presents no difficult search path.

4. **Compensation Technique**
   A technique to compute compensation waveforms for a linear transmission path has been developed. The path between the PEC and the DUT is modelled using a SFG technique. The model contains both lumped, and distributed circuit elements, each of which is represented by S-parameters. Methods to obtain the overall transfer function of the transmission path have been demonstrated.

   Examples of matched and mismatched channels were presented. Simulation results show that edge-placement accuracy and waveform quality at the DUT input pin can be significantly improved in both cases.

9.3 RECOMMENDATIONS FOR FURTHER RESEARCH

The research reported in this thesis investigated the feasibility of the proposed calibration method. Final implementation requires further investigation in the following areas:

1. **Frequency Domain Reflectometry**
   The major requirement is to develop a detector circuit to perform magnitude and phase measurement. One method, suggested in section 3.2, is to use a peak detector to measure only the magnitude, and then compute the phase information with the aid of a transmission line hybrid transformer. We obtain the sum (V_i+V_r) and difference $(V_i - V_r)$ vectors from the incident (V_i) and reflected (V_r) waves. Their magnitudes, $|V_i|, |V_r|, |V_i + V_r|$, and $|V_i - V_r|$, can be used to compute the phase angle between V_i and V_r using the well-known cosines law.

2. **Thickfilm-Hybrid Directional Coupler**
   The second prototype, the dual directional coupler, is suitable for this application. However, adjustment for optimum performance is required because of the demands of such high accuracy. Using a matched directional coupler minimizes main line signal degradation and maximizes measurement accuracy.

   Because TFH directional couplers have relatively high conductor losses due to the irregular shape of the centre conductor cross section, conductor lines should be fabricated by printing the substrate with photo-resist material using the negative of the layout, then printing conductor paste onto the entire substrate. Subsequent firing will burn away the photo-resist material, leaving a more nearly rectangular conductor cross section. Thinfilm technology is a possible alternative in this application, but availability and accessibility is limited.

3. **Optimization Technique**
   No further research should be required to seek a better optimization algorithm because the objective function is cooperative. Most optimization algorithms should work, but any difference would be principally in speed and memory requirement. Further investigation should be directed towards application of this technique to measuring the reflection coefficient of typical DUTs.

4. **Compensation Technique**
   Implementation with a real PEC is a desirable goal. An experiment with an actual PEC and DUT requires a high speed sampling oscilloscope to observe waveforms in the transmission path. Each part of the channel should be characterized by an automatic network analyzer to obtain the S-parameters to the neccessary accuracy. The method described in this thesis is a general one which may easily be modified and applied to different transmission paths. Pending the design and test of a practical PEC–DUT channel, it would be premature to make firm predictions regarding the ultimate value of this work.

APPENDIX A

ANALYSIS OF DIRECTIONAL ELECTROMAGNETIC COUPLERS

The material in section 5.1 requires some concepts and expressions for the general treatment of the directional coupling action of ordinary transmission lines. Appropriate basic results have been developed by OLIVER [1954] and most of the material given in this appendix follows that development. The assumptions used here for the transmission line characteristics are the same as in chapter 5.

A.1 NORMAL MODES AND LINE CONSTANTS

The propagation of waves on two parallel lines, such as shown in Figure A.1, is described by the set of differential equations

$$\begin{aligned}
\frac{\partial e_1}{\partial z} + L_{11}\frac{\partial i_1}{\partial t} + L_M\frac{\partial i_2}{\partial t} &= 0 \\
\frac{\partial i_1}{\partial z} + C_{11}\frac{\partial e_1}{\partial t} - C_M\frac{\partial e_2}{\partial t} &= 0 \\
\frac{\partial e_2}{\partial z} + L_{22}\frac{\partial i_2}{\partial t} + L_M\frac{\partial i_1}{\partial t} &= 0 \\
\frac{\partial i_2}{\partial z} + C_{22}\frac{\partial e_2}{\partial t} - C_M\frac{\partial e_1}{\partial t} &= 0
\end{aligned} \qquad \text{(A.1)}$$

where $L_{jj}, C_{jj}(j = 1, 2)$ are the self inductance and capacitance per unit length of line j, in the present of line $k(k = 2, 1)$ taking e_k and i_k to be zero, L_M is the mutual inductance per unit length and C_M is the mutual capacitance per unit length.

A particularly simple set of solutions is obtained by solving this set of simultaneous linear differential equations. There are four normal modes (two for each direction) characterized by fixed ratios of e_2/e_1 and i_2/i_1 which do not change as the wave propagates. In the normal mode equal power is associated with each line. The modes are characterized by:

$$\frac{e_2}{e_1} = \pm\sqrt{\frac{L_{22}}{L_{11}}} = \pm\sqrt{\frac{C_{11}}{C_{22}}} \qquad \text{(A.2)}$$

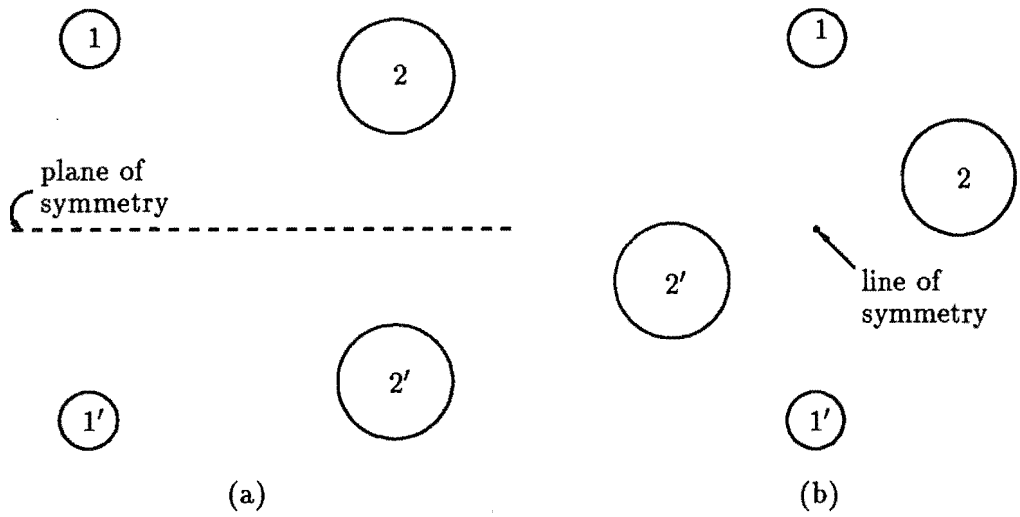


Figure A.1 Coupled balanced lines (a) lateral excitation (b) diagonal excitation.

and

$$e_1 i_1 = e_2 i_2 \tag{A.3}$$

The choice of the plus corresponds to *lateral* excitation in Figure A.1 (a), the minus sign to *diagonal* excitation Figure A.1 (b).

Substituting equation A.2 and A.3 into equation A.1 and letting

$$\begin{aligned} K_C &= \frac{C_M}{\sqrt{C_{11}C_{22}}} \\ K_L &= \frac{L_M}{\sqrt{L_{11}L_{22}}} \end{aligned} \tag{A.4}$$

equation A.1 is reduced to the familiar transmission line equations

$$\begin{aligned} \frac{\partial e_j}{\partial z} + L_{jj}(1 \pm K_L)\frac{\partial i_j}{\partial t} &= 0 \\ \frac{\partial i_j}{\partial z} + C_{jj}(1 \mp K_C)\frac{\partial e_j}{\partial t} &= 0 \end{aligned} \tag{A.5}$$

where $j = 1, 2$.

The velocity of propagation

$$v_p = \frac{1}{\sqrt{L_{jj}C_{jj}(1 \pm K_L)(1 \mp K_C)}} \tag{A.6}$$

must be the same for all modes, whether the upper signs or lower signs are selected. This can only be true if $K_L = K_C = K$. Hence for natural isotropic coupling

$$\frac{L_M}{C_M} = \sqrt{\frac{L_{11}L_{22}}{C_{11}C_{22}}} \tag{A.7}$$

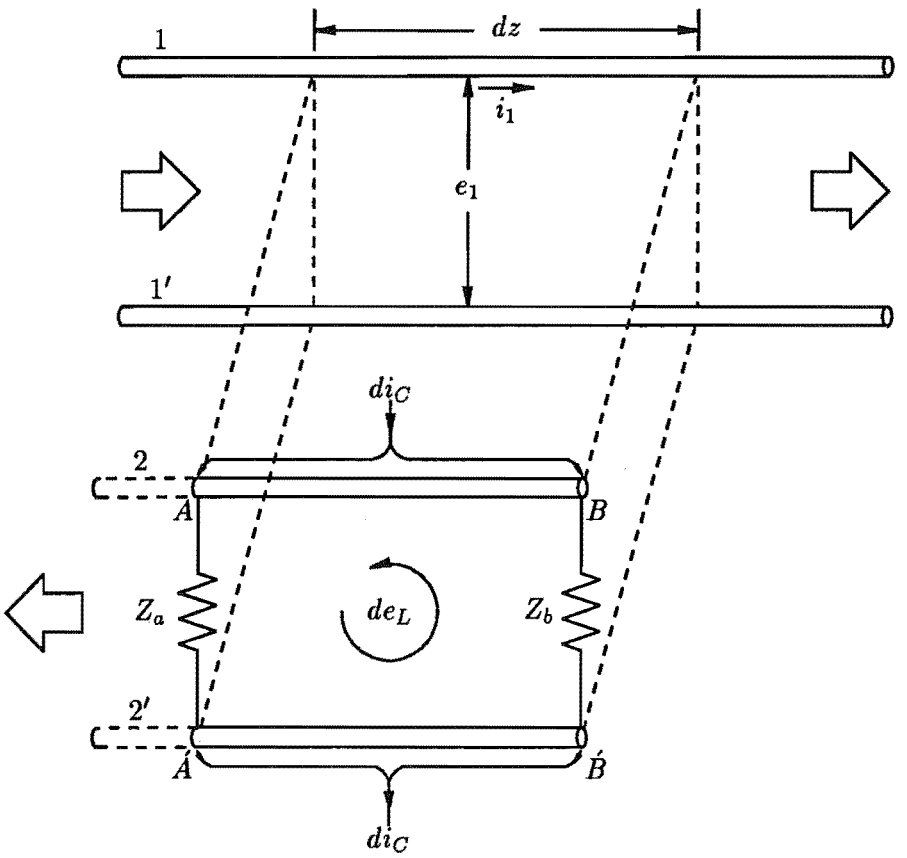


Figure A.2 A coupled elemental length of line.

and

$$v_p = \frac{1}{\sqrt{L_{jj}C_{jj}(1-K^2)}} \tag{A.8}$$

Since v_p must be independent of K, $L_{jj}C_{jj}$ must vary as $(1-K^2)^{-1}$.

A.2 NATURAL DIRECTIONAL COUPLING

Assume a wave is travelling from left to right in line 1 and consider the induced voltage and current produced in an elemental length dz of line 2 terminated with Z_a and Z_b as shown on Figure A.2.

The rising voltage on line 1 will produce the displacement current $di_C = \dfrac{\partial C_M e_1}{\partial t} dz$ while the increasing current in line 1 will produce the emf $de_L = \dfrac{\partial L_M i_1}{\partial t} dz$ around the loop as shown in Figure A.2. The total voltage across terminal $B\acute{B}$ will be:

$$\begin{aligned} de_{B\acute{B}} &= \frac{Z_a Z_b}{Z_a + Z_b} di_C - \frac{Z_b}{Z_a + Z_b} de_L \\ &= \frac{Z_b}{Z_a + Z_b} \frac{\partial}{\partial t} (Z_a C_M e_1 - L_M i_1) dz \end{aligned} \tag{A.9}$$

This voltage will be zero if

$$Z_a = \frac{L_M i_1}{C_M e_1} \tag{A.10}$$

but

$$\frac{i_1}{e_1} = \sqrt{\frac{C_{11}}{L_{11}}} \tag{A.11}$$

while from equation A.7

$$\frac{L_M}{C_M} = \sqrt{\frac{L_{11}L_{22}}{C_{11}C_{22}}}$$

From equations A.7, A.10, and A.11 give the value of Z_a

$$Z_a = \sqrt{\frac{L_{22}}{C_{22}}} \tag{A.12}$$

which is the characteristic impedance of line 2. So if we extend line 2 an arbitary distance to the left and terminate it with Z_a, the voltage $B\acute{B}$ will still be zero. This follows because the induction in each added elemental section produces no voltage or current at its right hand terminals. The entire induced voltage and current in each elemental section appear at the left and are of proper polarity to launch a wave travelling to the left. Any voltage or current appearing at the right is a result of reflection. The natural coupling between lines is therefore inherently directional. In particular it is *contra-directional*.

APPENDIX B

ANALYSIS OF PARALLEL-COUPLED TEM MODE TRANSMISSION LINES

This appendix gives an analysis of the steady-state response of parallel-coupled transmission lines, described in section 5.1. Most of the material given in this appendix follows that developed in the book by EDWARDS [1981, appendix A, pp. 165–171]. The assumptions for characteristics of the transmission line are the same as in chapter 5.

B.1 EVEN- AND ODD-MODE OF PROPAGATION

Any parallel-coupled pair of transmission lines, regardless of their practical realization, can be described by the four-port configuration indicated schematically in Figure B.1.

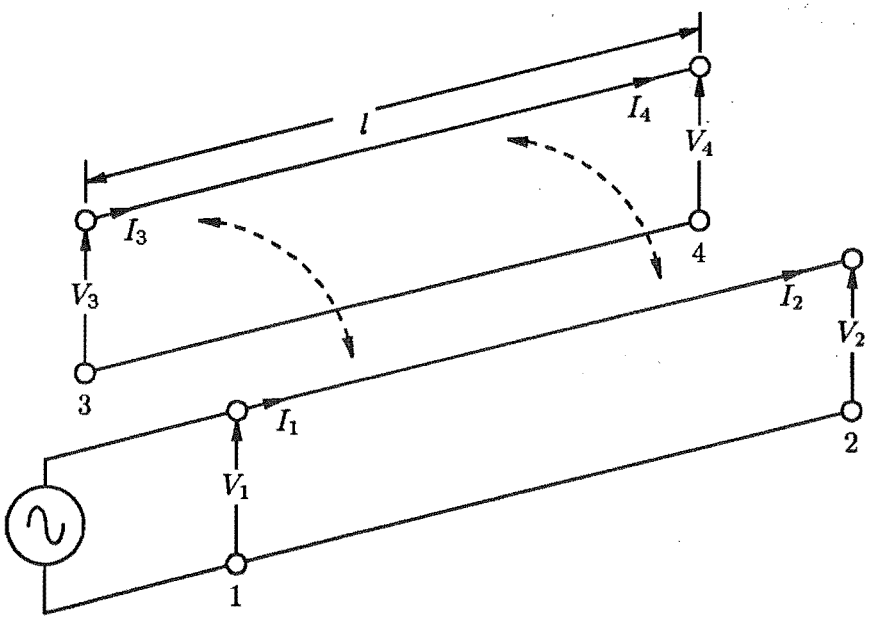


Figure B.1 Two parallel-coupled transmission lines.

At any instant the relative polarities of voltages, taken at any specific plane along

the structure, will either be alike or opposite. The different field configurations set up by such polarities are refered to as the *even-mode* and the *odd-mode* respectively. Figure B.2 illustrates these effects. The complete behavior of the coupled structure can be obtained by superposition of the effects due to those two modes.

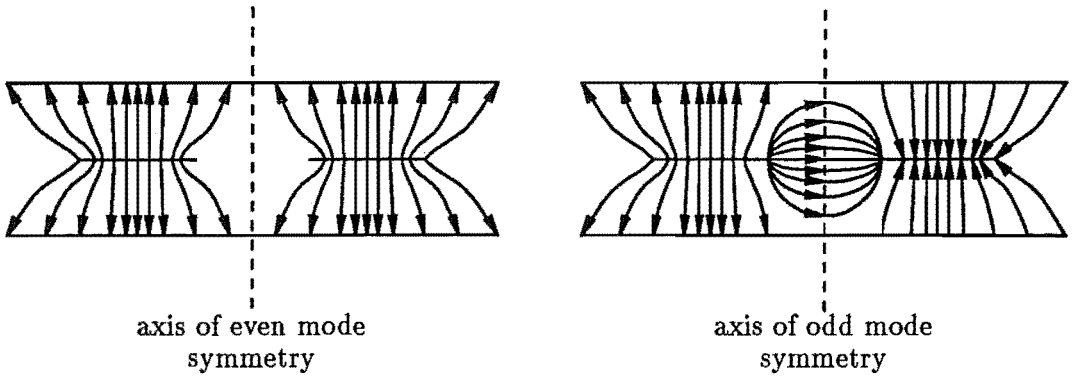


Figure B.2 Even-mode and odd-mode for two parallel-coupled lines.

Because of the assumed uniform dielectric filling, any signal travelling in such a pure TEM mode system will always travel at the same velocity, $v_p = c/\sqrt{\varepsilon_r}$. Thus the velocity associated with the even-mode is identical to that associated with the odd-mode.

The equivalent primary constants for the coupled lines having even- or odd-modes, taken separately, must differ bacause of the different field distributions. As a result of this two distinct characteristic impedances can be defined. The even-mode characteristic impedance, denoted by Z_{oe}, and the odd-mode characteristic impedances, denoted by Z_{oo}. This applies to any TEM mode or quasi-TEM mode parallel-coupled structure, and the characteristic impedances are major parameters in design procedures.

B.2 ANALYSIS FOR VOLTAGE AND CURRENT AT EACH PORT

The configuration in Figure B.1 can be analyzed by connecting matched terminations Z_0 at ports 2, 3, and 4, and driving the circuit at port 1 with a 2 V source having an impedance which is also equal to Z_0. The matched configuration is shown in Figure B.3.

The arrangement of Figure B.3 may be analyzed by first considering excitation under even-mode alone, then odd-mode condition alone, and finally combining the results. The notation is given in Figure B.4.

Since the structure is physically symmetrical, it can be seen that only 2 circuits, Figures B.4 (a)(ii) and (b)(ii) need be solved. Then, the total voltages and currents on the original structure are a superposition of the even- and odd-mode solutions as

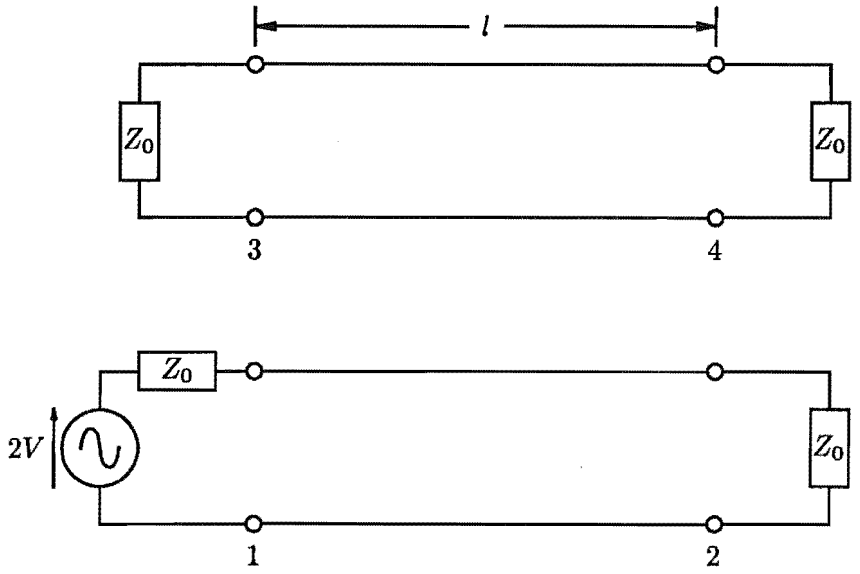


Figure B.3 Matched parallel-coupled transmission lines.

follows:

$$\begin{aligned} V_1 &= V_{1e} + V_{1o} \\ V_2 &= V_{2e} + V_{2o} \\ V_3 &= V_{1e} - V_{1o} \\ V_4 &= V_{2e} - V_{2o} \end{aligned} \tag{B.1}$$

$$\begin{aligned} I_1 &= I_{1e} + I_{1o} \\ I_2 &= I_{2e} + I_{2o} \\ I_3 &= I_{1e} - I_{1o} \\ I_4 &= I_{2e} - I_{2o} \end{aligned} \tag{B.2}$$

The voltage and current relations for lines (a)(ii) and (b)(ii) are expressed by the ABCD matrix as follows:

$$\begin{bmatrix} V_{1e} \\ I_{1e} \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_{oe}\sin\theta \\ jY_{oe}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_{2e} \\ I_{2e} \end{bmatrix} \tag{B.3}$$

and

$$\begin{bmatrix} V_{1o} \\ I_{1o} \end{bmatrix} = \begin{bmatrix} \cos\theta & jZ_{oo}\sin\theta \\ jY_{oo}\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_{2o} \\ I_{2o} \end{bmatrix} \tag{B.4}$$

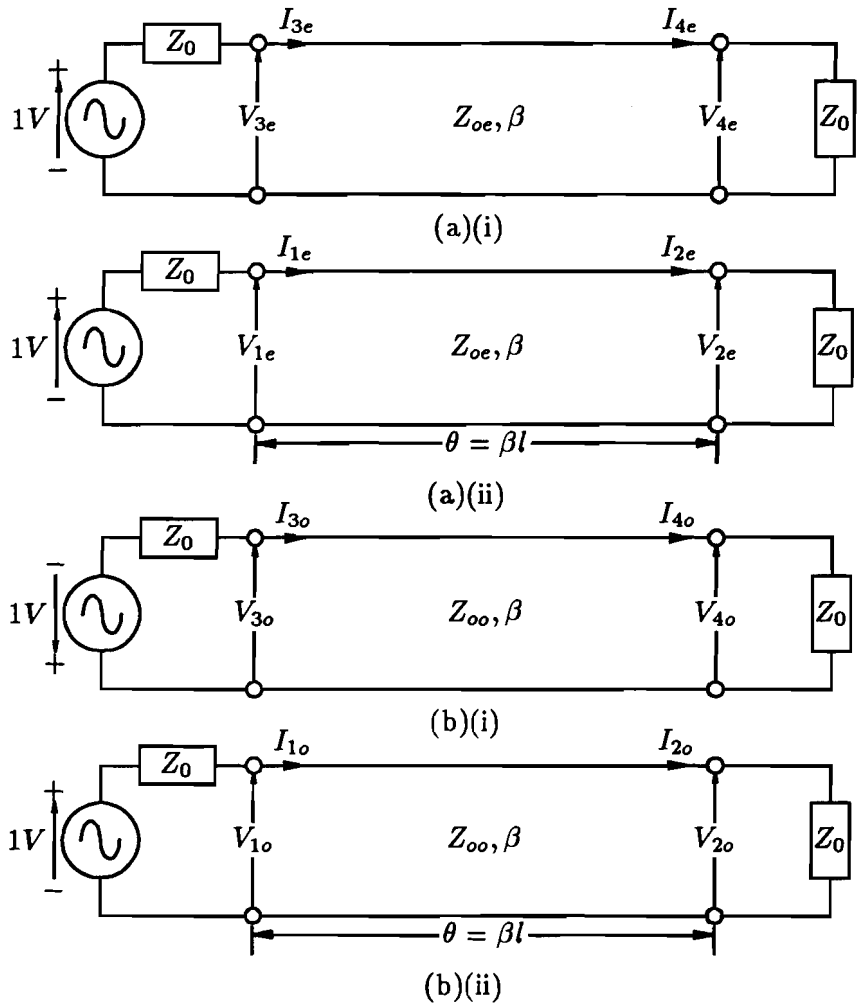


Figure B.4 Separated even and odd mode equivalent circuits for the parallel-coupled transmission lines (a) even-mode (b) odd-mode.

Applying the terminal conditions $V_{2e} = Z_0 I_{2e}, V_{2o} = Z_0 I_{2o}, V_{1e} + I_{1e} Z_0 = 1$ and $V_{1o} + I_{1o} Z_0 = 1$ results in the voltage and current expressions:

$$V_{1e} = \frac{Z_{oe} Z_0 \cos\theta + jZ_{oe}^2 \sin\theta}{2Z_{oe} Z_0 \cos\theta + j(Z_{oe}^2 + Z_0^2)\sin\theta} \tag{B.5}$$

$$I_{1e} = \frac{Z_{oe} \cos\theta + jZ_0 \sin\theta}{2Z_{oe} Z_0 \cos\theta + j(Z_{oe}^2 + Z_0^2)\sin\theta} \tag{B.6}$$

$$V_{2e} = \frac{Z_{oe} Z_0}{2Z_{oe} Z_0 \cos\theta + j(Z_{oe}^2 + Z_0^2)\sin\theta} \tag{B.7}$$

$$I_{2e} = \frac{Z_{oe}}{2Z_{oe} Z_0 \cos\theta + j(Z_{oe}^2 + Z_0^2)\sin\theta} \tag{B.8}$$

$$V_{1o} = \frac{Z_{oo} Z_0 \cos\theta + jZ_{oo}^2 \sin\theta}{2Z_{oo} Z_0 \cos\theta + j(Z_{oo}^2 + Z_0^2)\sin\theta} \tag{B.9}$$

$$I_{1o} = \frac{Z_{oo}\cos\theta + jZ_0\sin\theta}{2Z_{oo}Z_0\cos\theta + j(Z_{oo}^2 + Z_0^2)\sin\theta} \tag{B.10}$$

$$V_{2o} = \frac{Z_{oo}Z_0}{2Z_{oo}Z_0\cos\theta + j(Z_{oo}^2 + Z_0^2)\sin\theta} \tag{B.11}$$

$$I_{2o} = \frac{Z_{oo}}{2Z_{oo}Z_0\cos\theta + j(Z_{oo}^2 + Z_0^2)\sin\theta} \tag{B.12}$$

The next step contains an important simplification which amounts to forcing the composite original circuit to become matched to the feed lines of characteristic impedance Z_0. Therefore, the total input impedance must equal Z_0:

$$\begin{aligned} Z_{in} &= Z_0 \\ &= \frac{V_1}{I_1} \\ &= \frac{V_{1e} + V_{1o}}{I_{1e} + I_{1o}} \end{aligned} \tag{B.13}$$

Substituting equations B.5, B.6, B.9 and B.10 into B.13 gives

$$Z_0 = \frac{Z_0(Z_{oo}D_e + Z_{oe}D_o)\cos\theta + j(Z_{oo}^2D_e + Z_{oe}^2D_o)\sin\theta}{(Z_{oo}D_e + Z_{oe}D_o)\cos\theta + jZ_0(D_e + D_o)\sin\theta} \tag{B.14}$$

where

$$D_e = 2Z_{oe}Z_0\cos\theta + j(Z_{oe}^2 + Z_0^2)\sin\theta$$

and

$$D_o = 2Z_{oo}Z_0\cos\theta + j(Z_{oo}^2 + Z_0^2)\sin\theta$$

The equality (equation B.14) will be established if

$$Z_0^2(D_e + D_o) = Z_{oo}^2D_e + Z_{oe}^2D_o \tag{B.15}$$

Substituing D_e and D_o into equation B.14, results in

$$\begin{aligned} 2Z_0^3(Z_{oo} + Z_{oe})\cos\theta + j(Z_{oe}^2Z_0^2 + Z_{oo}^2Z_0^2 + 2Z_0^4)\sin\theta \;=\; \\ 2Z_{oe}Z_{oo}Z_0(Z_{oo} + Z_{oe})\cos\theta + j(Z_{oe}^2Z_0^2 + Z_{oo}^2Z_0^2 + 2Z_{oe}^2Z_{oo}^2)\sin\theta \end{aligned} \tag{B.16}$$

This equality will be satisfied if

$$Z_0^2 = Z_{oe}Z_{oo} \tag{B.17}$$

Inserting this relationship into equations B.9 to B.12 gives:

$$V_{1e} = \frac{Z_0\cos\theta + jZ_{oe}\sin\theta}{2Z_0\cos\theta + j(Z_{oe} + Z_{oo})\sin\theta} \tag{B.18}$$

$$I_{1e} = \frac{\cos\theta + jZ_{oo}Y_0\sin\theta}{2Z_0\cos\theta + j(Z_{oe} + Z_{oo})\sin\theta} \tag{B.19}$$

$$V_{2e} = \frac{Z_0}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.20}$$

$$I_{2e} = \frac{1}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.21}$$

$$V_{1o} = \frac{Z_0\cos\theta + jZ_{oo}\sin\theta}{2Z_0\cos\theta + j(Z_{oo}+Z_{oe})\sin\theta} \tag{B.22}$$

$$I_{1o} = \frac{\cos\theta + jZ_{oe}Y_0\sin\theta}{2Z_0\cos\theta + j(Z_{oo}+Z_{oe})\sin\theta} \tag{B.23}$$

$$V_{2o} = \frac{Z_0}{2Z_0\cos\theta + j(Z_{oo}+Z_{oe})\sin\theta} \tag{B.24}$$

$$I_{2o} = \frac{1}{2Z_0\cos\theta + j(Z_{oo}+Z_{oe})\sin\theta} \tag{B.25}$$

Final expressions for the total (complete structure) voltages and currents can now be obtained by substituting equations B.18 to B.25 into group of equations B.1 and B.2:

$$V_1 = \frac{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})sin\theta} \tag{B.26}$$

$$V_2 = \frac{2Z_0}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.27}$$

$$V_3 = \frac{j(Z_{oe}-Z_{oo})\sin\theta}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.28}$$

$$V_4 = \frac{0}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.29}$$

$$I_1 = \frac{2\cos\theta + jY_0(Z_{oe}+Z_{oo})\sin\theta}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.30}$$

$$I_2 = \frac{2}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.31}$$

$$I_3 = \frac{jY_0(Z_{oo}-Z_{oe})\sin\theta}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.32}$$

$$I_4 = \frac{0}{2Z_0\cos\theta + j(Z_{oe}+Z_{oo})\sin\theta} \tag{B.33}$$

These voltages and currents can be further simplified by defining a coupling parameter K such that

$$K = \frac{Z_{oe}-Z_{oo}}{Z_{oe}+Z_{oo}} \tag{B.34}$$

This definition plus the relationship $Z_0^2 = Z_{oe}Z_{oo}$ allows us to write:

$$V_1 = 1 \tag{B.35}$$

$$V_2 = \frac{\sqrt{1-K^2}}{\sqrt{1-K^2}\cos\theta + j\sin\theta} \tag{B.36}$$

$$V_3 = \frac{jK\sin\theta}{\sqrt{1-K^2}\cos\theta + j\sin\theta} \tag{B.37}$$

$$V_4 = 0 \tag{B.38}$$

The maximum degree of coupling occurs when the length of the coupled structure is $\lambda/4$, or $\theta = \pi/2$. This condition, set into equations B.36 and B.37 yields:

$$V_2 = -j\sqrt{1-K^2} \tag{B.39}$$

$$V_3 = K \tag{B.40}$$

Equation B.40 gives the mid-band (maximum) extent of coupling K, expressed in terms of impedances by equation B.34. Equation B.39 shows that the transmitted voltage V_2 (not electromagnetically coupled) depends on K and is 90 degrees out-of-phase with V_1, and hence also V_3. This feature gives rise to the names often used for couplers based upon this parallel-coupled line principle; a *90° hybrid*, or a *quadrature* coupler.

APPENDIX C

BELLE AND CIF CODES FOR THE DIRECTIONAL COUPLER

The followings are BELLE and CIF codes for the layouts of the prototype directional couplers.

C.1 THE SINGLE DIRECTIONAL COUPLER

C.1.1 BELLE Codes for the Coupler

```
BEGIN {main}
COMMENT('This is the design of a single Directional Coupler ');
DEFINE ('Coupler');
  LAYER (cond1);
     Box (332,610,2708,621);
     Box (60,575,80,655);
     Box (2960,575,2980,655);
     Box (500,140,580,160);
     Box (2460,140,2540,160);
     Box (300,318,340,358);
     Box (260,358,300,398);
     Box (2700,318,2740,358);
     Box (2740,358,2780,398);
     Wire (11,540.5,389.5);dy(190);
     Wire (11,540.5,579.5);dx(1960);
     Wire (11,2500.5,389.5);dy(190);
     Wire (11,540.5,1460.5);dy(190);
     Wire (11,540.5,1460.5);dx(1960);
     Wire (11,2500.5,1460.5);dy(190);
     Wire (25,59.5,615.5);dx(267);
     Wire (25,2713.5,615.5);dx(267);
     Wire (25,539.5,139.5);dy(245);
```

```
    Wire (25,2500.5,139.5);dy(245);
    Wire (25,59.5,1424.5);dx(267);
    Wire (25,2713.5,1424.5);dx(267);
    Wire (25,540.5,1655.5);dy(245);
    Wire (25,2500.5,1655.5);dy(245);
    Box (332,1419,2708,1430);
    Box (60,1385,80,1465);
    Box (2960,1385,2980,1465);
    Box (500,1880,580,1900);
    Box (2460,1880,2540,1900);
    Box (300,1682,340,1722);
    Box (260,1642,300,1682);
    Box (2700,1682,2740,1722);
    Box (2740,1642,2780,1682);
 LAYER (cond2);
    Box (0,575,80,655);
    Box (2960,575,3040,655);
    Box (500,0,580,160);
    Box (2460,0,2540,160);
    Box (785,0,2255,280);
    Box (600,180,2440,498);
    Box (0,1385,80,1465);
    Box (2960,1385,3040,1465);
    Box (500,1880,580,2040);
    Box (2460,1880,2540,2040);
    Box (785,1760,2255,2040);
    Box (600,1542,2440,1860);
    Box (340,698,2700,1342);
    Box (320,798,360,1242);
    Box (2680,798,2720,1242);
    Box (300,358,340,398);
    Box (2700,358,2740,398);
    Box (300,1642,340,1682);
    Box (2700,1642,2740,1682);
  LAYER (res1);
    Box (560,70,805,130);
    Box (2235,70,2480,130);
    Box (260,318,300,358);
    Box (2740,318,2780,358);
    Box (560,1910,805,1970);
    Box (2235,1910,2480,1970);
```

```
    Box (260,1682,300,1722);
    Box (2740,1682,2780,1722);
ENDDEF;
 DRAW ('Coupler',0,0);
END; {main}
```

C.1.2 BELLE Codes for the Ground Plane

```
BEGIN {main}
COMMENT('This is the design of groundplane ');
DEFINE ('groundplane');
  LAYER (cond1);
    Box (340,398,2700,798);
    Box (340,1242,2700,1642);
    Box (240,300,280,340);
    Box (200,340,240,380);
    Box (2760,300,2800,340);
    Box (2800,340,2840,380);
    Box (240,1700,280,1740);
    Box (200,1660,240,1700);
    Box (2760,1700,2800,1740);
    Box (2800,1660,2840,1700);
  LAYER (res1);
    Wire (40,400,448);dx(1);
    Wire (40,720,448);dx(1);
    Wire (40,1040,448);dx(1);
    Wire (40,1360,448);dx(1);
    Wire (40,1680,448);dx(1);
    Wire (40,2000,448);dx(1);
    Wire (40,2320,448);dx(1);
    Wire (40,2640,448);dx(1);
    Wire (40,400,748);dx(1);
    Wire (40,720,748);dx(1);
    Wire (40,1040,748);dx(1);
    Wire (40,1360,748);dx(1);
    Wire (40,1680,748);dx(1);
    Wire (40,2000,748);dx(1);
    Wire (40,2320,748);dx(1);
    Wire (40,2640,748);dx(1);
    Wire (40,400,1292);dx(1);
    Wire (40,720,1292);dx(1);
    Wire (40,1040,1292);dx(1);
```

```
      Wire (40,1360,1292);dx(1);
      Wire (40,1680,1292);dx(1);
      Wire (40,2000,1292);dx(1);
      Wire (40,2320,1292);dx(1);
      Wire (40,2640,1292);dx(1);
      Wire (40,400,1592);dx(1);
      Wire (40,720,1592);dx(1);
      Wire (40,1040,1592);dx(1);
      Wire (40,1360,1592);dx(1);
      Wire (40,1680,1592);dx(1);
      Wire (40,2000,1592);dx(1);
      Wire (40,2320,1592);dx(1);
      Wire (40,2640,1592);dx(1);
      Box (240,340,280,380);
      Box (2760,340,2800,380);
      Box (240,1660,280,1700);
      Box (2760,1660,2800,1700);
      Box (200,300,240,340);
      Box (2800,300,2840,340);
      Box (200,1700,240,1740);
      Box (2800,1700,2840,1740);
ENDDEF;
 DRAW ('groundplane',200,300);
END; {main}
```

C.1.3 CIF Codes for the Coupler

```
25 Lambda = 250;
(This is the design of a single Directional Coupler);
DS 1001;
9 Coupler;
42 0,0 760000,510000;
  L CP1;
B 594000 2750 380000,153875;
B 5000 20000 17500,153750;
B 5000 20000 742500,153750;
B 20000 5000 135000,37500;
B 20000 5000 625000,37500;
B 10000 10000 80000,84500;
B 10000 10000 70000,94500;
B 10000 10000 680000,84500;
B 10000 10000 690000,94500;
```

```
W 2750  135125,97375 135125,144875;
W 2750  135125,144875 625125,144875;
W 2750  625125,97375 625125,144875;
W 2750  135125,365125 135125,412625;
W 2750  135125,365125 625125,365125;
W 2750  625125,365125 625125,412625;
W 6250  14875,153875 81625,153875;
W 6250  678375,153875 745125,153875;
W 6250  134875,34875 134875,96125;
W 6250  625125,34875 625125,96125;
W 6250  14875,356125 81625,356125;
W 6250  678375,356125 745125,356125;
W 6250  135125,413875 135125,475125;
W 6250  625125,413875 625125,475125;
B 594000 2750 380000,356125;
B 5000 20000 17500,356250;
B 5000 20000 742500,356250;
B 20000 5000 135000,472500;
B 20000 5000 625000,472500;
B 10000 10000 80000,425500;
B 10000 10000 70000,415500;
B 10000 10000 680000,425500;
B 10000 10000 690000,415500;
  L CP2;
B 20000 20000 10000,153750;
B 20000 20000 750000,153750;
B 20000 40000 135000,20000;
B 20000 40000 625000,20000;
B 367500 70000 380000,35000;
B 460000 79500 380000,84750;
B 20000 20000 10000,356250;
B 20000 20000 750000,356250;
B 20000 40000 135000,490000;
B 20000 40000 625000,490000;
B 367500 70000 380000,475000;
B 460000 79500 380000,425250;
B 590000 161000 380000,255000;
B 10000 111000 85000,255000;
B 10000 111000 675000,255000;
B 10000 10000 80000,94500;
B 10000 10000 680000,94500;
```

```
B 10000 10000 80000,415500;
B 10000 10000 680000,415500;
  L R1;
B 61250 15000 170625,25000;
B 61250 15000 589375,25000;
B 10000 10000 70000,84500;
B 10000 10000 690000,84500;
B 61250 15000 170625,485000;
B 61250 15000 589375,485000;
B 10000 10000 70000,425500;
B 10000 10000 690000,425500;
DF;
C 1001 T 0,0;
End
```

C.1.4 CIF Codes for the Ground Plane

```
25 Lambda = 250;
(This is the design of groundplane);
DS 1001;
9 groundplane;
42 50000,75000 710000,435000;
  L CP1;
B 590000 100000 380000,149500;
B 590000 100000 380000,360500;
B 10000 10000 65000,80000;
B 10000 10000 55000,90000;
B 10000 10000 695000,80000;
B 10000 10000 705000,90000;
B 10000 10000 65000,430000;
B 10000 10000 55000,420000;
B 10000 10000 695000,430000;
B 10000 10000 705000,420000;
  L R1;
W 10000  100000,112000 100250,112000;
W 10000  180000,112000 180250,112000;
W 10000  260000,112000 260250,112000;
W 10000  340000,112000 340250,112000;
W 10000  420000,112000 420250,112000;
W 10000  500000,112000 500250,112000;
W 10000  580000,112000 580250,112000;
W 10000  660000,112000 660250,112000;
```

```
W 10000  100000,187000 100250,187000;
W 10000  180000,187000 180250,187000;
W 10000  260000,187000 260250,187000;
W 10000  340000,187000 340250,187000;
W 10000  420000,187000 420250,187000;
W 10000  500000,187000 500250,187000;
W 10000  580000,187000 580250,187000;
W 10000  660000,187000 660250,187000;
W 10000  100000,323000 100250,323000;
W 10000  180000,323000 180250,323000;
W 10000  260000,323000 260250,323000;
W 10000  340000,323000 340250,323000;
W 10000  420000,323000 420250,323000;
W 10000  500000,323000 500250,323000;
W 10000  580000,323000 580250,323000;
W 10000  660000,323000 660250,323000;
W 10000  100000,398000 100250,398000;
W 10000  180000,398000 180250,398000;
W 10000  260000,398000 260250,398000;
W 10000  340000,398000 340250,398000;
W 10000  420000,398000 420250,398000;
W 10000  500000,398000 500250,398000;
W 10000  580000,398000 580250,398000;
W 10000  660000,398000 660250,398000;
B 10000 10000 65000,90000;
B 10000 10000 695000,90000;
B 10000 10000 65000,420000;
B 10000 10000 695000,420000;
B 10000 10000 55000,80000;
B 10000 10000 705000,80000;
B 10000 10000 55000,430000;
B 10000 10000 705000,430000;
DF;
C 1001 T 50000,75000;
End
```

C.2 THE DUAL DIRECTIONAL COUPLER

C.2.1 BELLE Codes

```
BEGIN {main}
COMMENT('This is the design of a Dual Directional Coupler ');
```

```
set45;
DEFINE ('Coupler');
  LAYER (cond1);
     Wire (12,66,533);dx(1440);
     Wire (12,1506,533);dxy(250,250);dy(240);
     Wire (12,1966,507);dx(-1440);
     Wire (12,526,507);dxy(-326,-326);dy(-40);
     Box (1987,25,2007,45);
     Box (2007,5,2027,25);
  LAYER (cond2);
     Box (5,517,45,547);
     Box (1987,493,2027,523);
     Wire (30,40,533);dx(20);
     Wire (30,1992,507);dx(-20);
     Box (193,15,207,150);
     Box (5,5,125,125);
     Box (275,5,395,125);
     Box (375,15,1927,27);
     Box (15,105,27,400);
     Box (2005,105,2017,400);
     Box (1907,5,1967,75);
     Box (1090,5,1210,65);
     Box (1907,65,2027,125);
     Box (2005,630,2017,980);
     Box (1967,940,2027,1025);
     Box (15,656,27,980);
     Box (5,940,65,1025);
     Box (2007,25,2027,45);
   LAYER (res1);
     Box (110,15,290,115);
     Box (50,517,60,547);
     Box (1972,493,1982,523);
     Box (1987,5,2007,25);
   LAYER (diel1); <-- This layer is for the ground plane
     Box (5,115,2027,1050);
     Box (5,5,125,165);
     Box (275,5,2027,165);
ENDDEF;
 DRAW ('Coupler',0,0);
 DRAW ('Coupler',0,2032);my;
END; {main}
```

C.2.2 CIF Codes

```
25 Lambda = 250;
(This is the design of a Dual Directional Coupler);
DS 1001;
9 Coupler;
42 1250,1250 506750,262500;
L CP1;
W 3000  16500,133250 376500,133250;
W 3000  376500,133250 439000,195750 439000,255750;
W 3000  491500,126750 131500,126750;
W 3000  131500,126750 50000,45250 50000,35250;
B 5000 5000 499250,8750;
B 5000 5000 504250,3750;
L CP2;
B 10000 7500 6250,133000;
B 10000 7500 501750,127000;
W 7500  10000,133250 15000,133250;
W 7500  498000,126750 493000,126750;
B 3500 33750 50000,20625;
B 30000 30000 16250,16250;
B 30000 30000 83750,16250;
B 388000 3000 287750,5250;
B 3000 73750 5250,63125;
B 3000 73750 502750,63125;
B 15000 17500 484250,10000;
B 30000 15000 287500,8750;
B 30000 15000 491750,23750;
B 3000 87500 502750,201250;
B 15000 21250 499250,245625;
B 3000 81000 5250,204500;
B 15000 21250 8750,245625;
B 5000 5000 504250,8750;
L R1;
B 45000 25000 50000,16250;
B 2500 7500 13750,133000;
B 2500 7500 494250,127000;
B 5000 5000 499250,3750;
L DP1;
B 505500 233750 254000,145625;
B 30000 40000 16250,21250;
```

```
B 438000 40000 287750,21250;
DF;
C 1001 T 0,0;
C 1001 MY T 0,508000;
End
```

APPENDIX D

DIRECTIONAL COUPLERS' S-PARAMETERS

This appendix gives the reflection coefficients of the prototype couplers, and the necessary S-parameters of the HP778D Dual Directional Coupler. All these S-parameters were measured using a HP8510 Automatic Network Analyzer over the frequency range of 100 MHz to 1 GHz at 20 MHz intervals.

D.1 MEASUREMENT CONFIGURATIONS

The measurement configuration for S_{ii} where $i = 1, \ldots, 4$ is illustrated in Figure D.1.

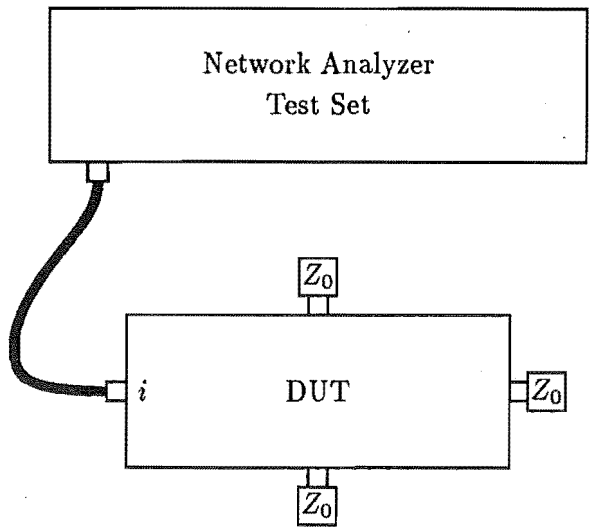


Figure D.1 ANA S-parameters measurement circuit for S_{ii}.

The measurement configuration for S_{ij} $(i \neq j)$ where $i = 1, \ldots, 4$ and $j = 1, \ldots, 4$, is shown in Figure D.2. The reciprocity and symmetry are assumed, but this assumption has not been verified (i. e. only S_{21}, S_{31}, and S_{41} have been measured).

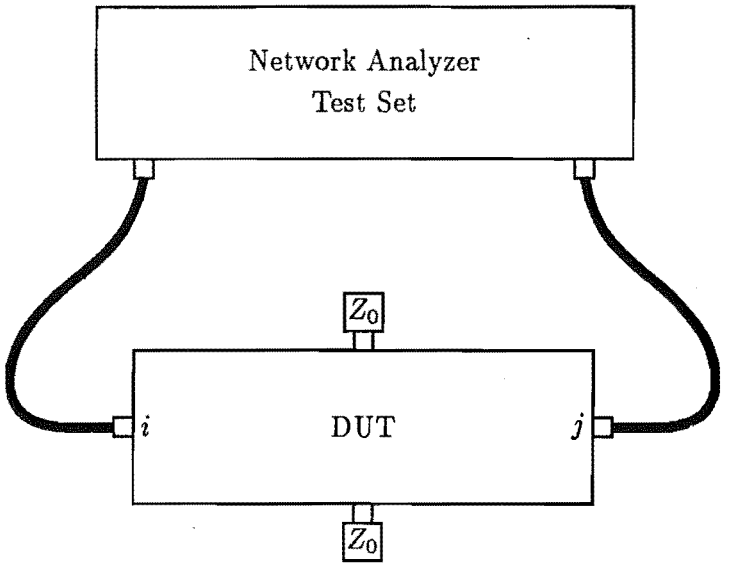


Figure D.2 ANA S-parameters measurement circuit for S_{ij}.

D.2 THE PROTOTYPE DIRECTIONAL COUPLERS

D.2.1 The Reflection Coefficient

The reflection coefficients of each port, for the single and dual directional couplers, are plotted in Figures D.3 to D.4 and Figures D.5 to D.6 respectively.

D.3 THE HP778D DUAL DIRECTIONAL COUPLER

The HP778D's S-parameters are included for comparison purposes. Port notation is the same as that for the prototype couplers.

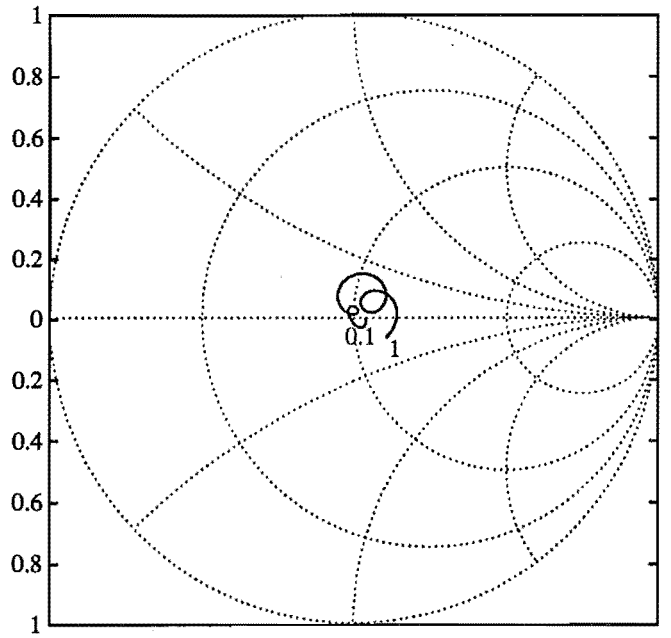
This 50 Ω coaxial dual directional coupler has a frequency range from 100 MHz to 2 GHz with a nominal coupling factor of −20 dB.

D.3.1 The Reflection Coefficient

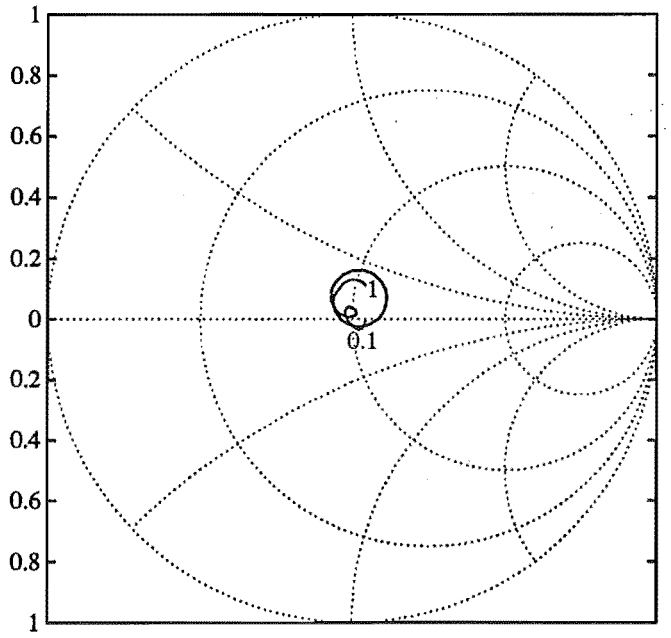
The reflection coefficients for each port of the HP778D are given in Figures D.7 to D.8.

D.3.2 The Transmission, Coupling, and Isolation Factors

The transmission, coupling, and isolation factors are plotted in Figures D.9 to D.11 respectively.

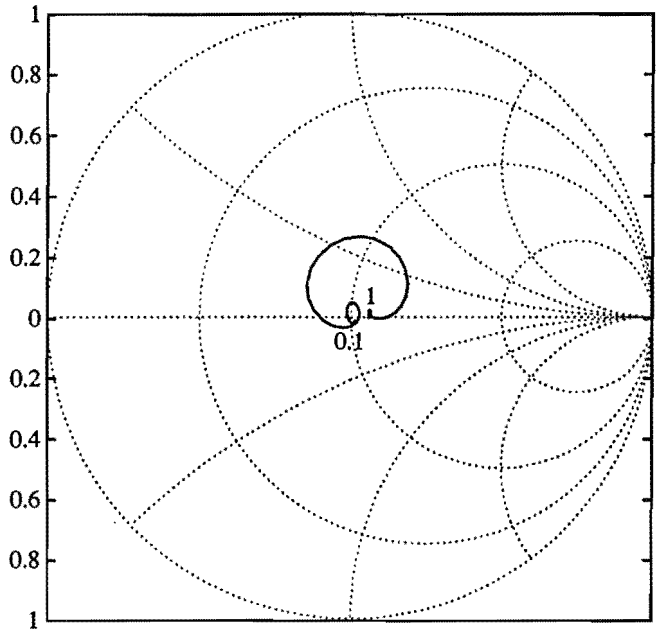


(a)

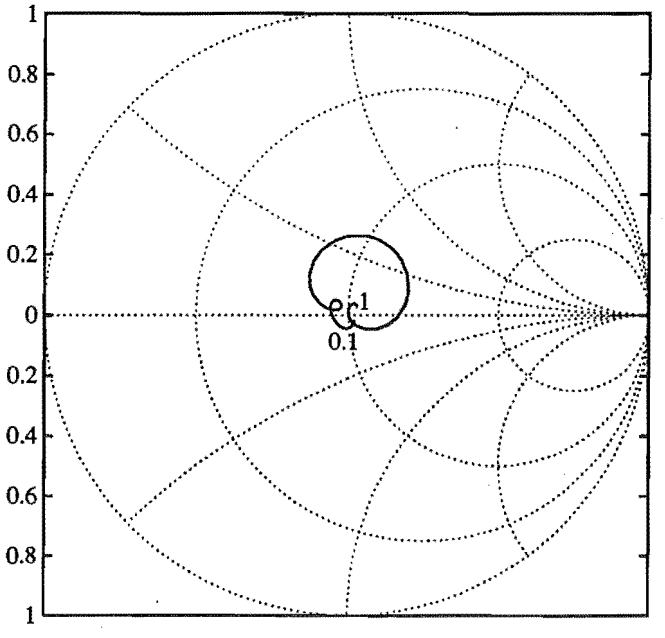


(b)

Figure D.3 The reflection coefficients of the single directional coupler (a) S_{11} (b) S_{22}.

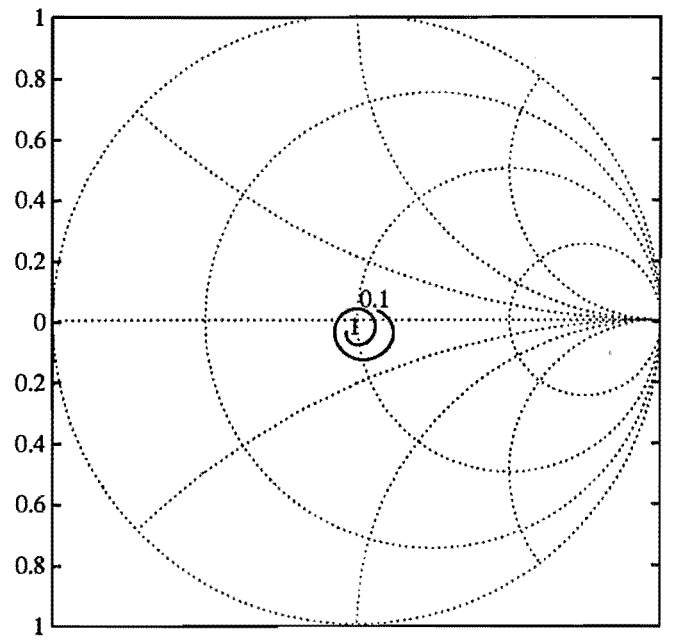


(a)

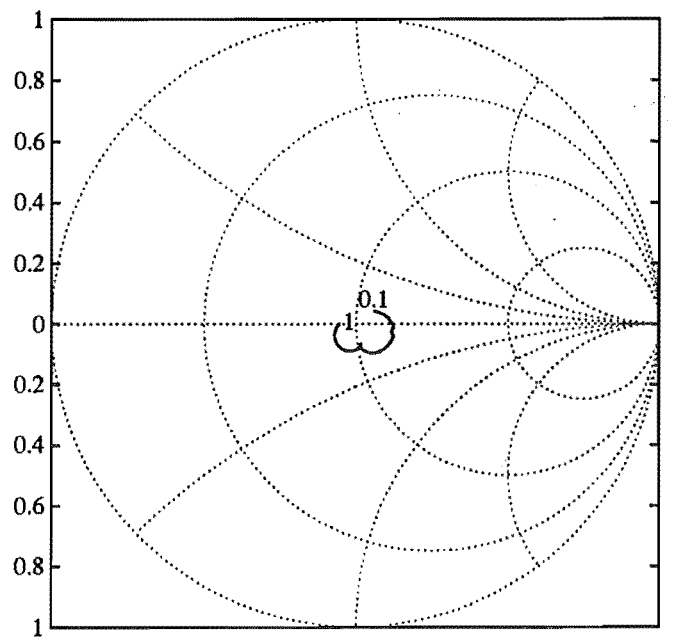


(b)

Figure D.4 The reflection coefficients of the single directional coupler (a) S_{33} (b) S_{44}.

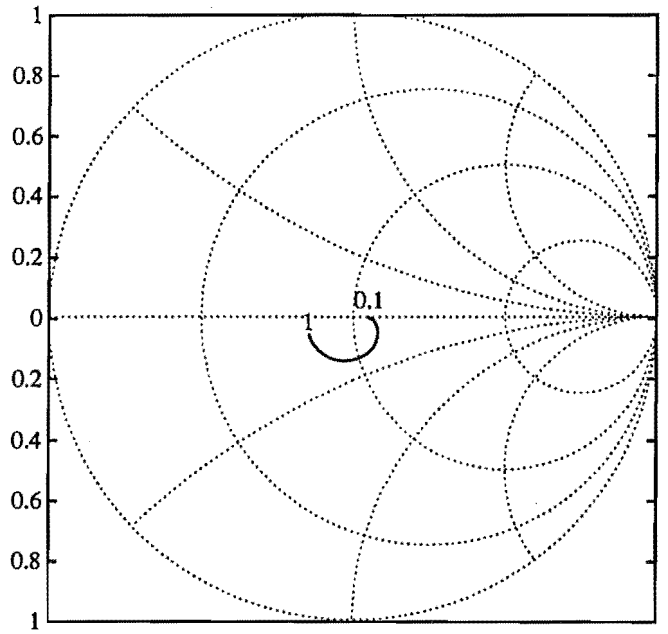


(a)

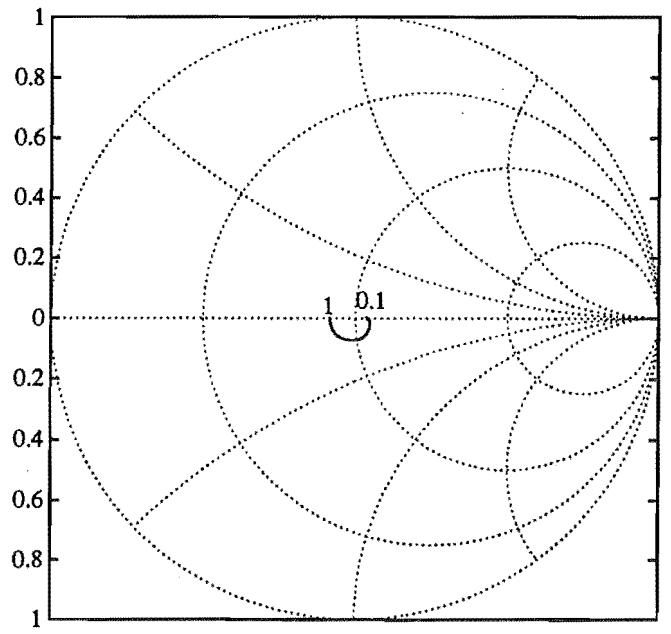


(b)

Figure D.5 The reflection coefficients of the dual directional coupler (a) S_{11} (b) S_{22}.

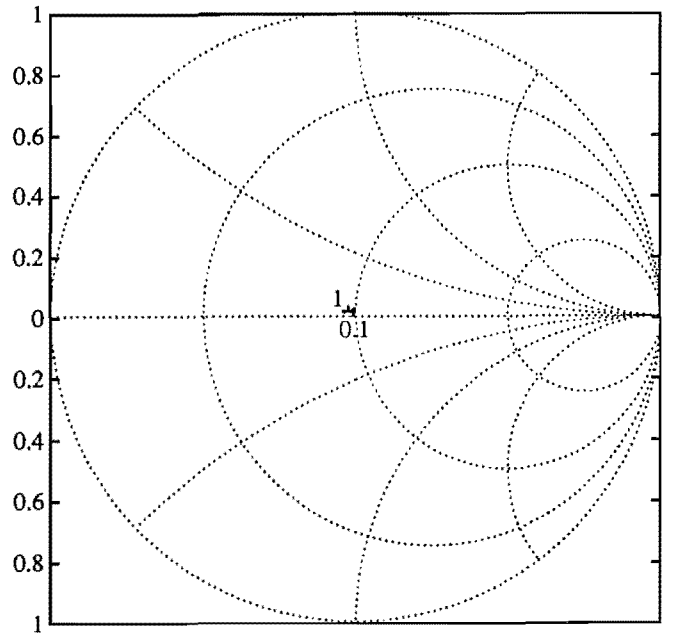


(a)

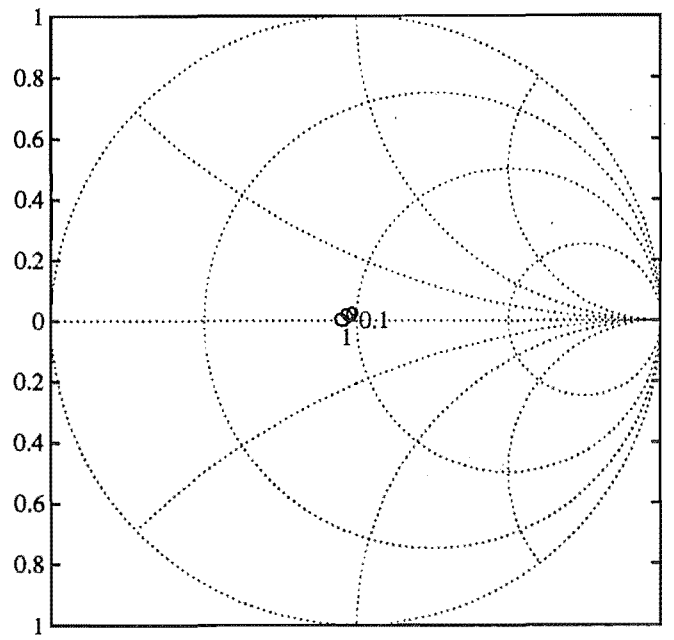


(b)

Figure D.6 The reflection coefficients of the dual directional coupler (a) S_{33} (b) S_{44}.

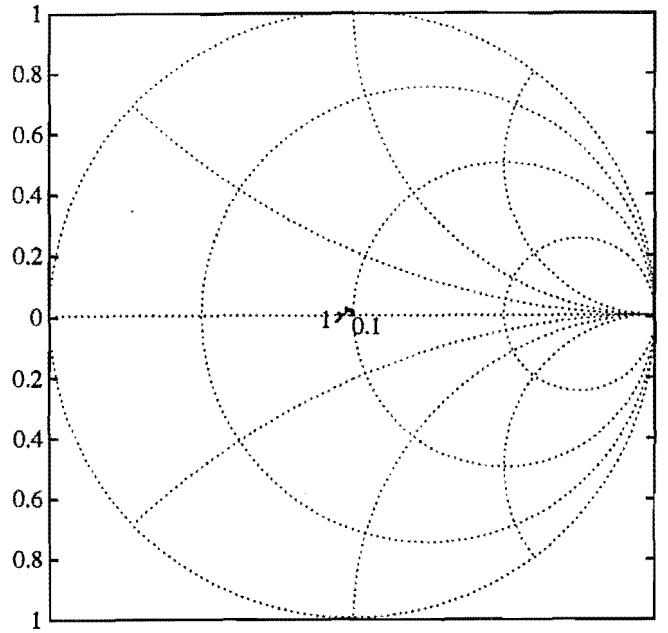


(a)

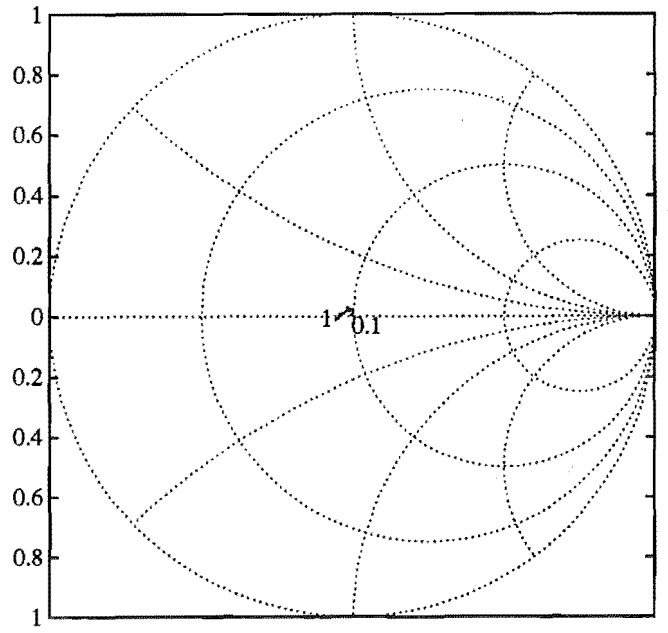


(b)

Figure D.7 HP778D reflection coefficients (a) S_{11} (b) S_{22}.



(a)



(b)

Figure D.8 HP778D reflection coefficients (a) S_{33} (b) S_{44}.

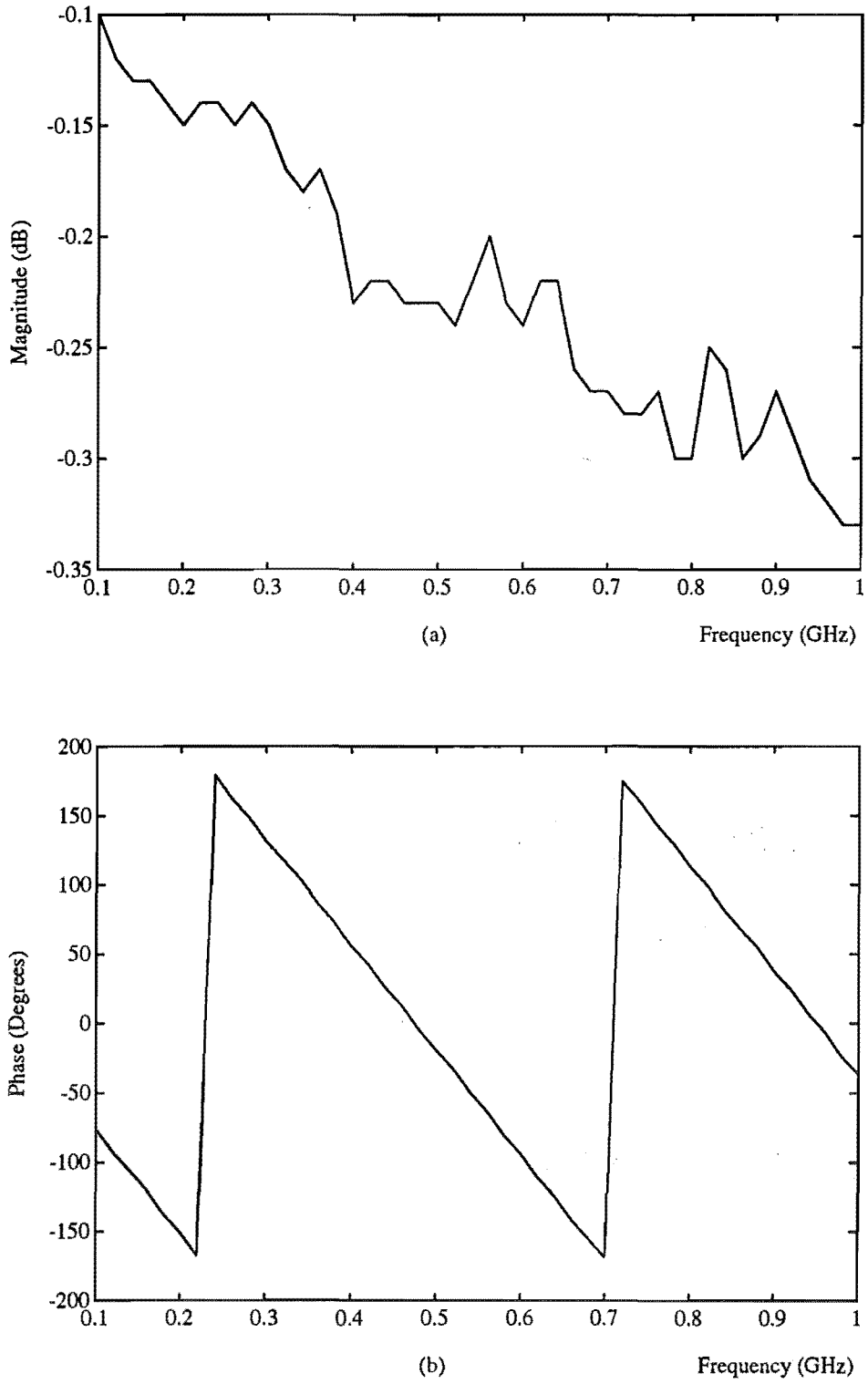


Figure D.9 HP778D transmission factor ($S_{12} = S_{21}$) (a) magnitude (b) phase.

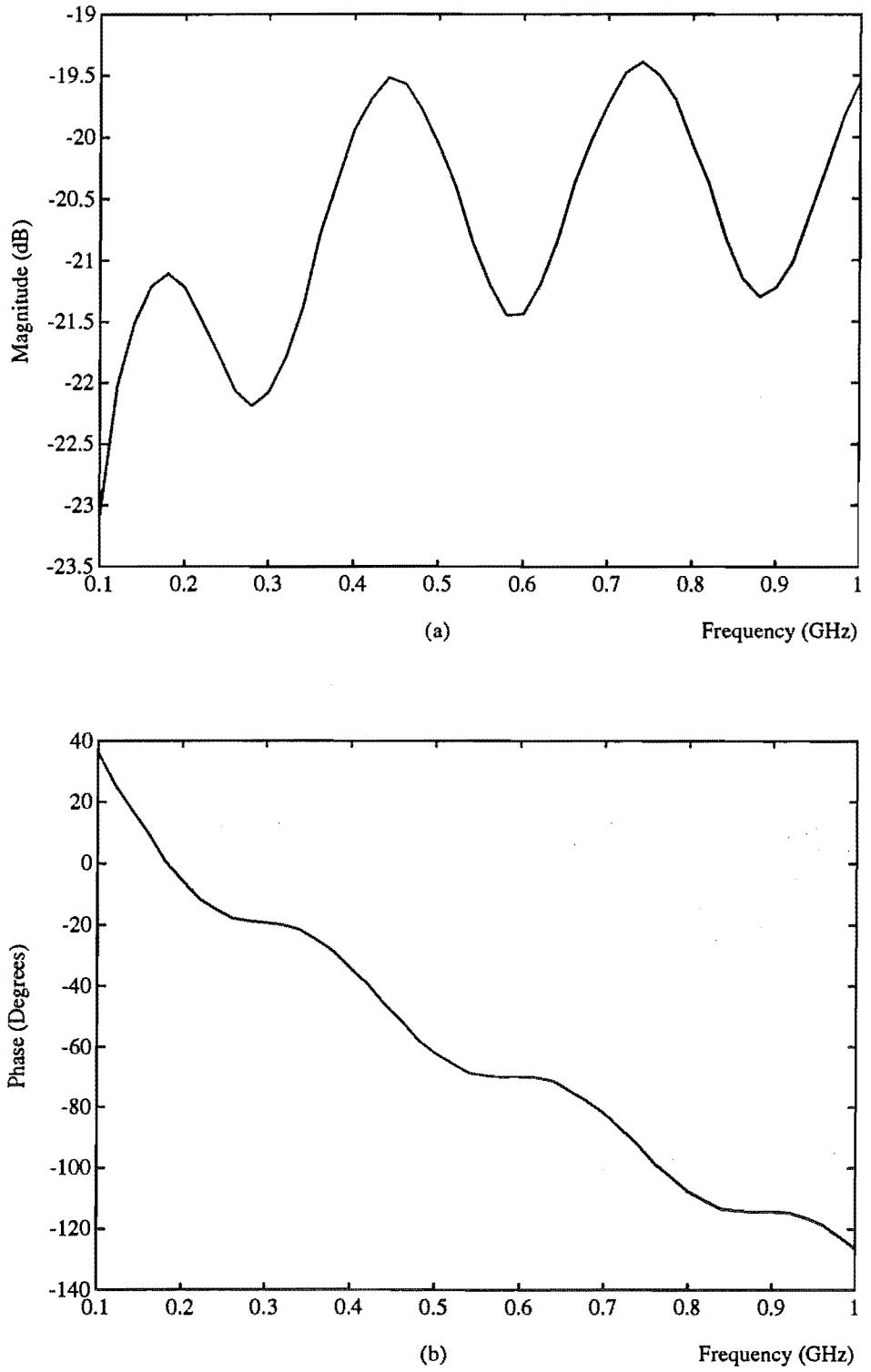


Figure D.10 HP778D coupling factor ($S_{13} = S_{31} = S_{24} = S_{42}$) (a) magnitude (b) phase.

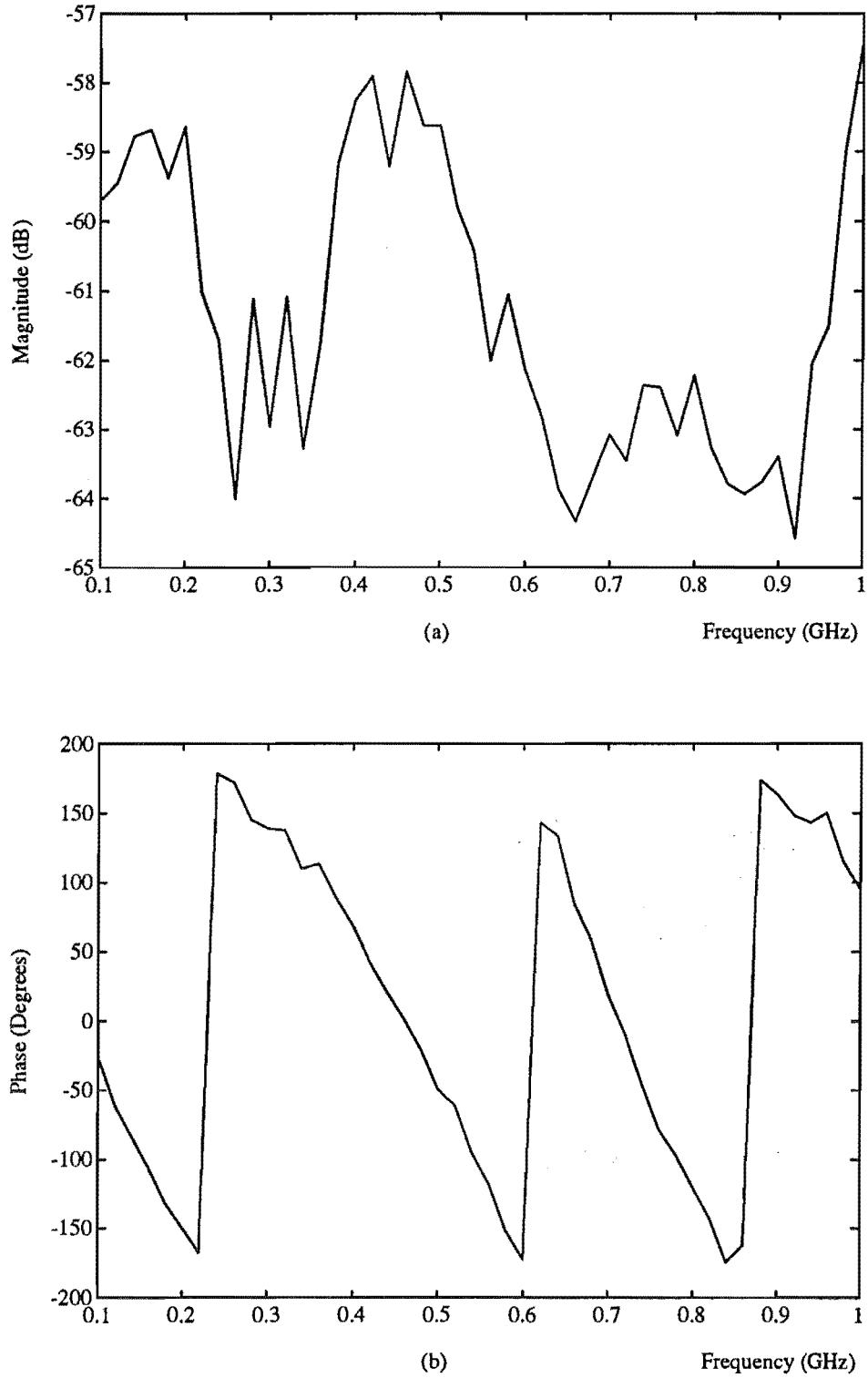


Figure D.11 HP778D isolation factor ($S_{14} = S_{41} = S_{23} = S_{32}$) (a) magnitude (b) phase.

APPENDIX E

FDR RESULTS FOR THE TFH DIRECTIONAL COUPLERS

This appendix gives the reflection coefficients of the loads (illustrated in Figure 6.1, section 6.1) measured using the prototype directional couplers. The measurement configuration and all the assumptions are the same as those described in section 6.2. The frequency range is from 100 MHz to 1 GHz at 100 MHz intervals.

Because all the loads are passive and have only positive real part, their reflection coefficient magnitudes must be less than or equal to 1. When the reflection coefficient magnitudes are larger than 1, the cause is measurement uncertainty.

E.1 THE SINGLE DIRECTIONAL COUPLER RESULTS

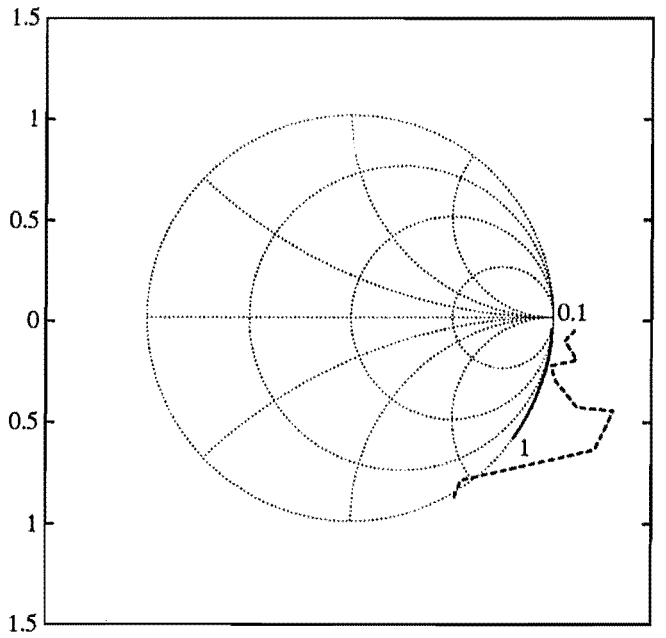
The FDR results obtained using the single directional coupler are plotted in Figures E.1 to E.3 for the capacitive loads; Figures E.4 to E.6 for the inductive loads; Figures E.7 to E.11 for the resistive loads. For clarity of the comparison, the FDR results for R_3 to R_6 are plotted separately from the ANA results.

The solid line is the result from the HP 8510 Automatic Network Analyzer; dashed line is the result from the single directional coupler.

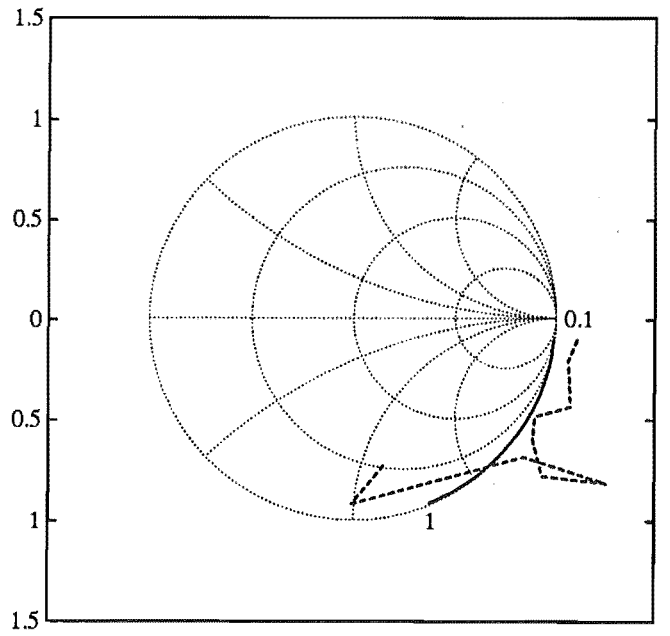
E.2 THE DUAL DIRECTIONAL COUPLER RESULTS

The FDR results obtained using the dual directional coupler are plotted in Figures E.12 to E.14 for the capacitive loads; Figures E.15 to E.17 for the inductive loads; Figures E.18 to E.22 for the resistive loads. For clarity of the comparison, the FDR results for R_3 to R_6 are plotted separately from the ANA results.

The solid line is the result from the HP 8510 Automatic Network Analyzer; dashed line is the result from the dual directional coupler.

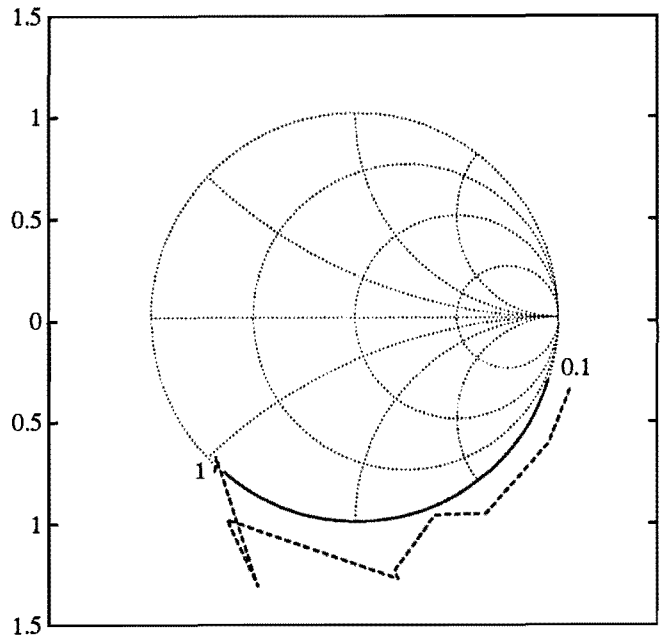


(a)

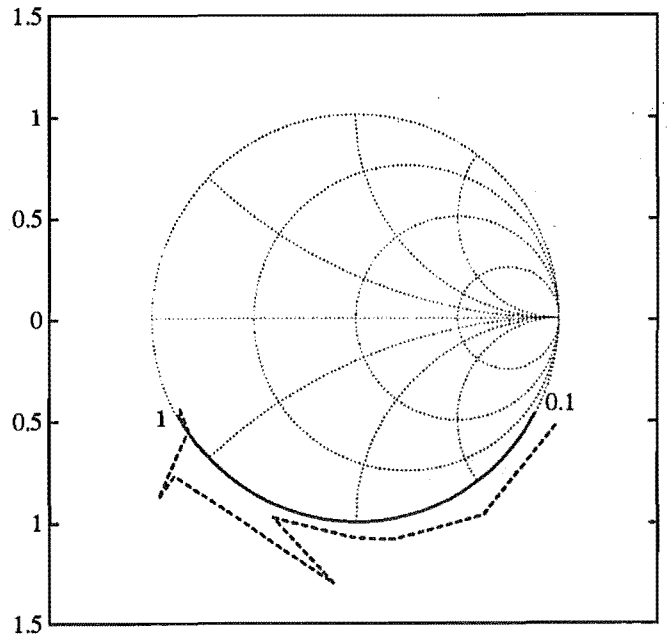


(b)

Figure E.1 FDR measurement results for (a) C_1: 1 pF (b) C_2: 2.2 pF.

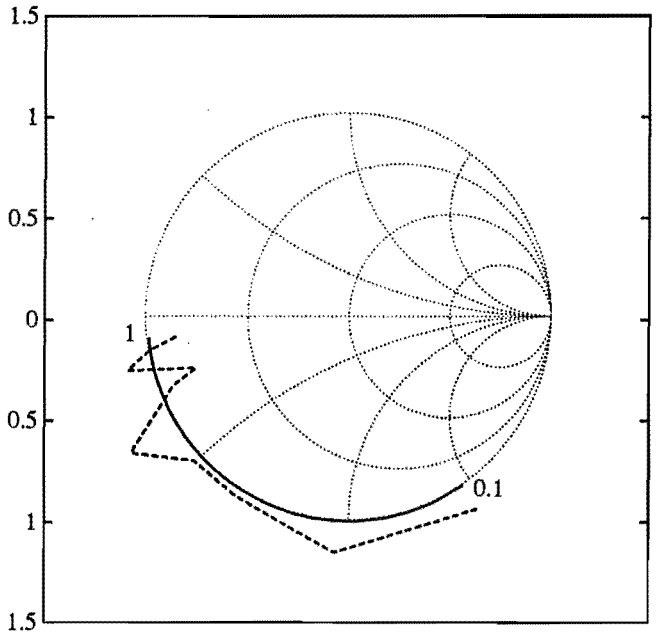


(a)

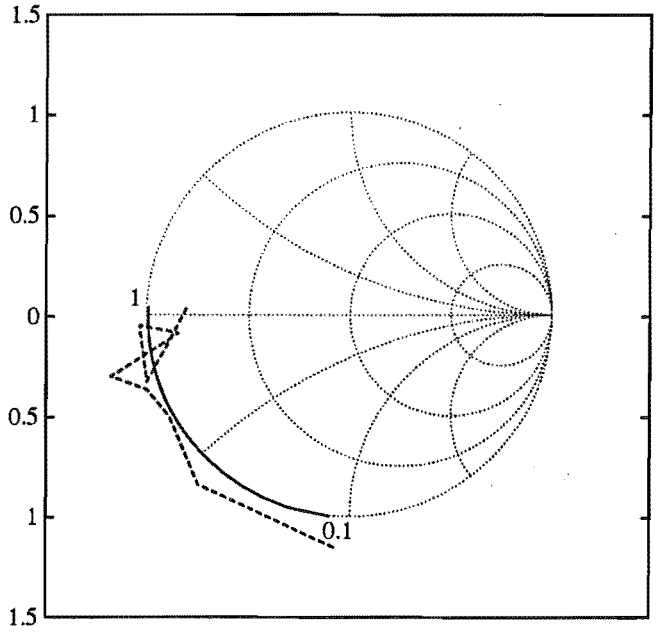


(b)

Figure E.2 FDR measurement results for (a) C_3: 4.7 pF (b) C_4: 8.2 pF.

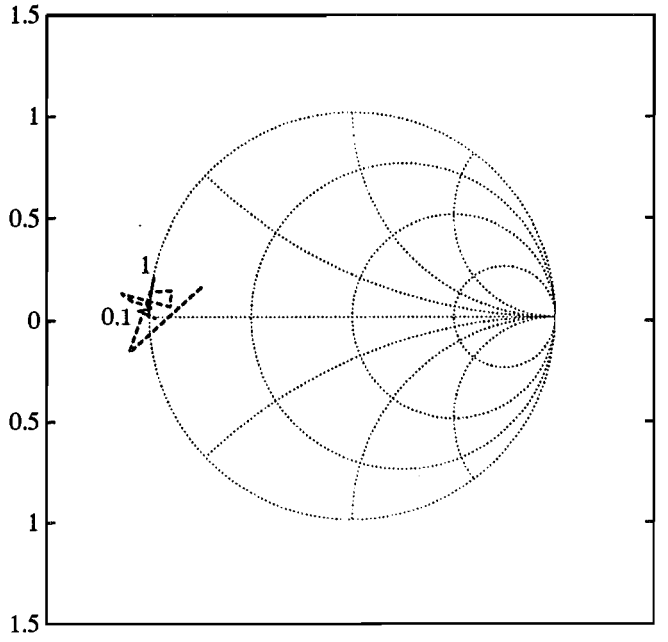


(a)

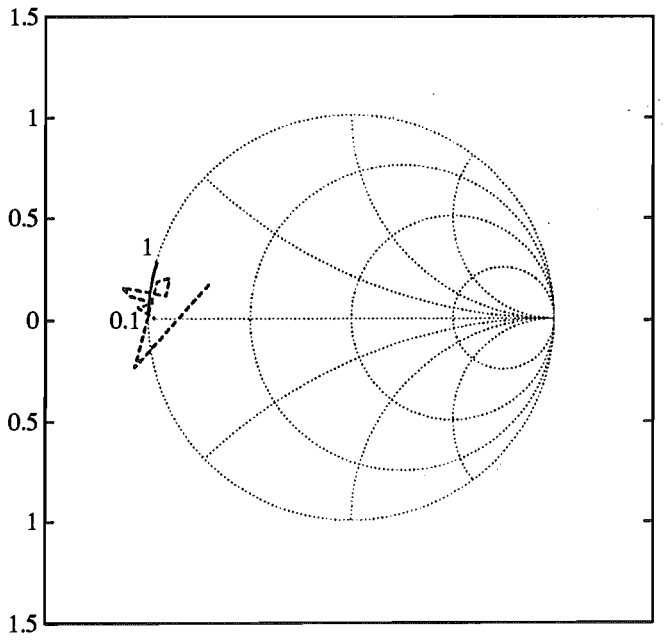


(b)

Figure E.3 FDR measurement results for (a) C_5: 18 pF (b) C_6: 33 pF.

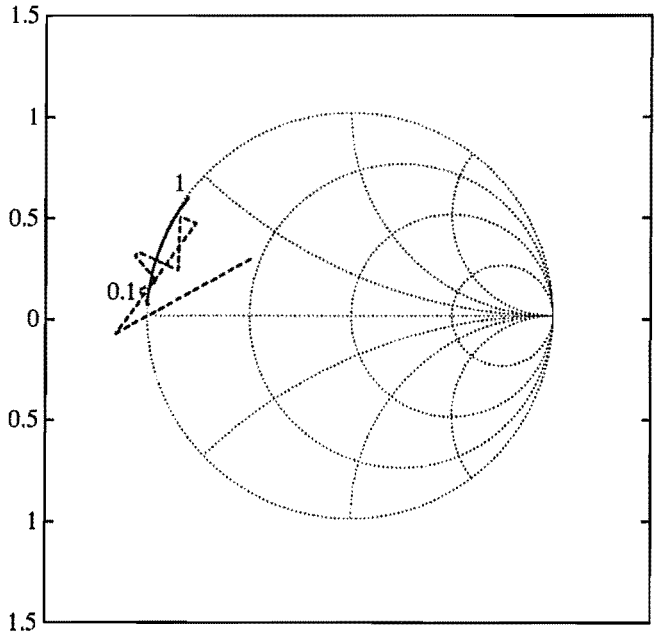


(a)

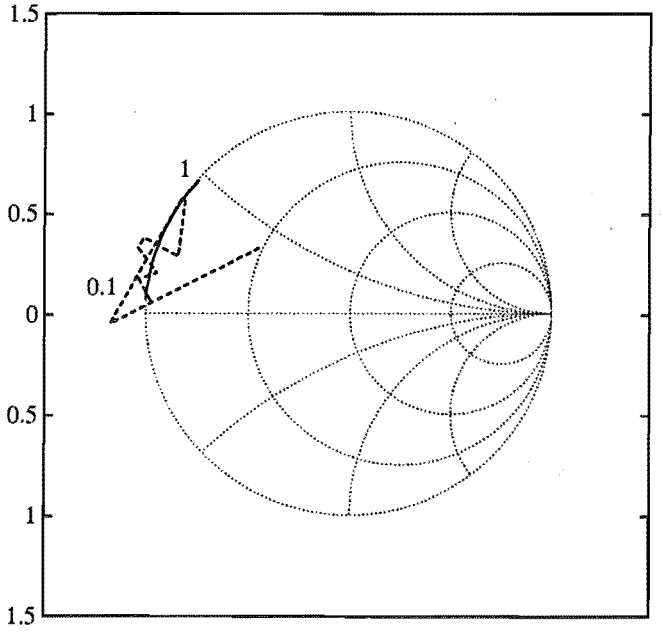


(b)

Figure E.4 FDR measurement results for (a) L_1: 0.68 nH (b) L_2: 1.92 nH.

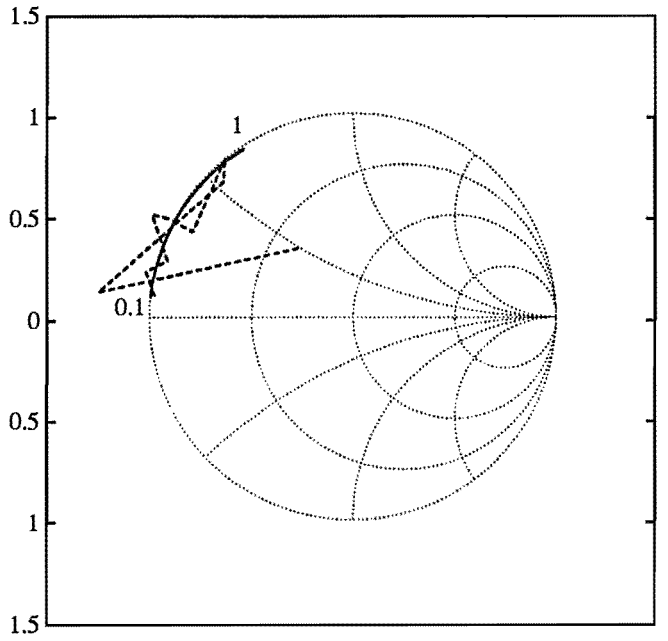


(a)

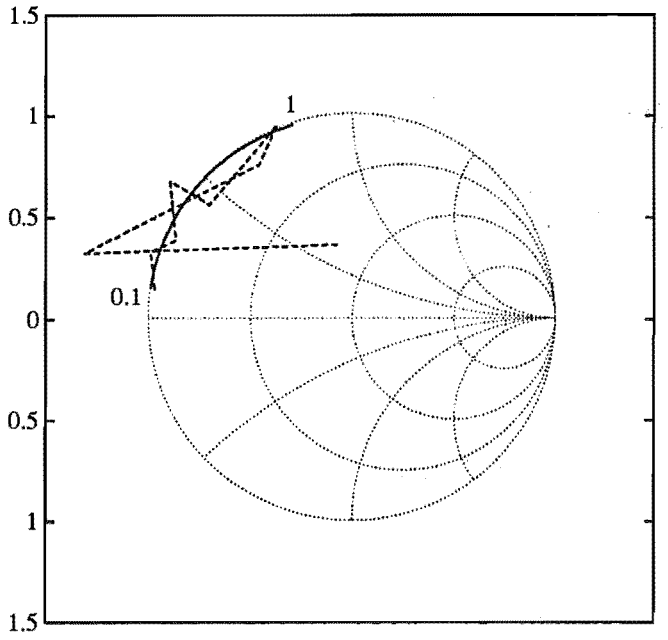


(b)

Figure E.5 FDR measurement results for (a) L_3: 3.37 nH (b) L_4: 4.95 nH.

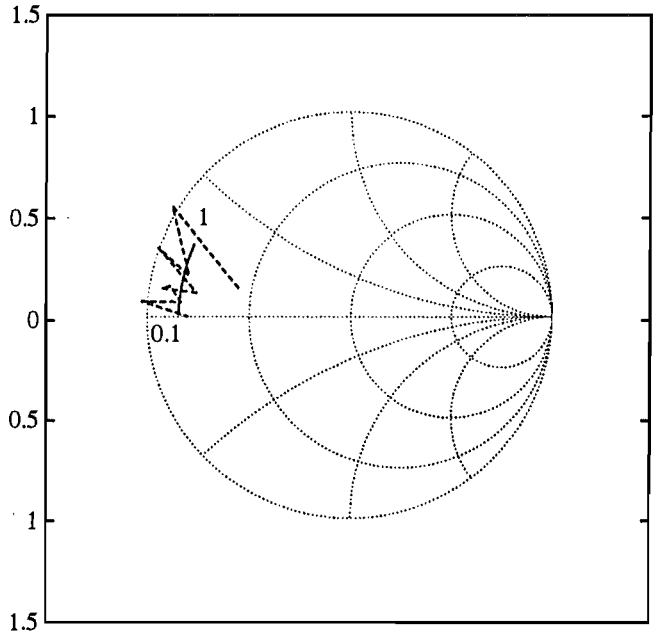


(a)

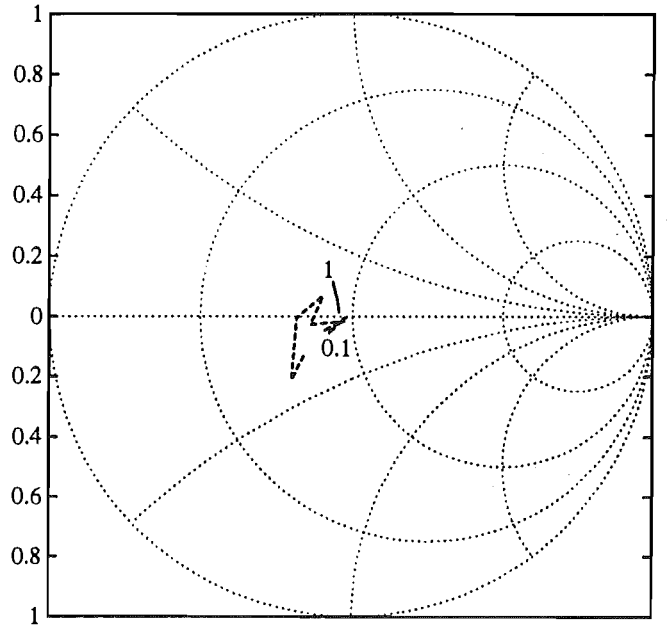


(b)

Figure E.6 FDR measurement results for (a) L_5: 6.63 nH (b) L_6: 8.4 nH.

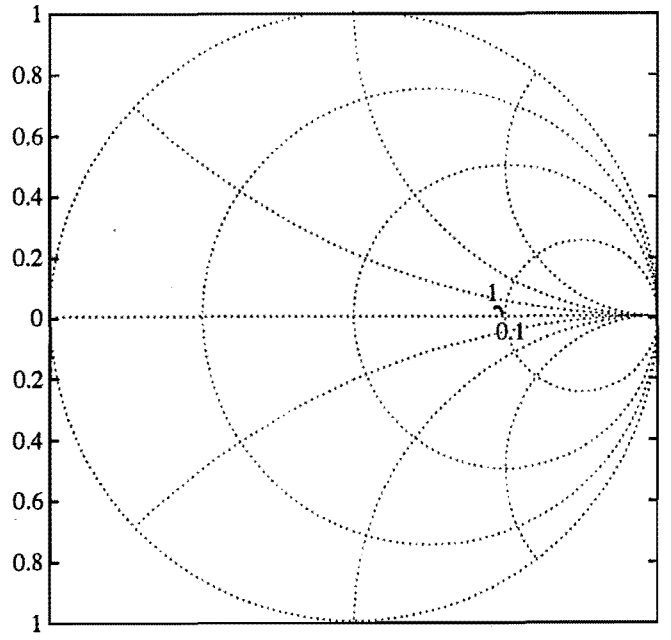


(a)

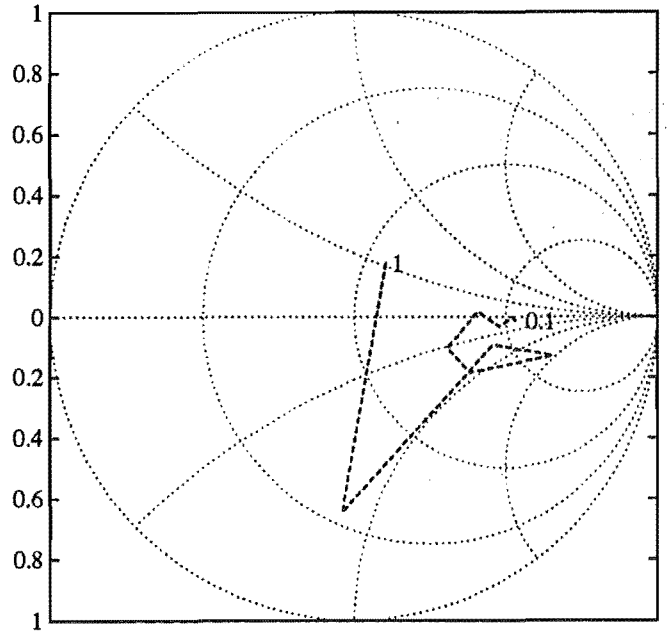


(b)

Figure E.7 FDR measurement results for (a) R_1: 4.4Ω (b) R_2: 46Ω.

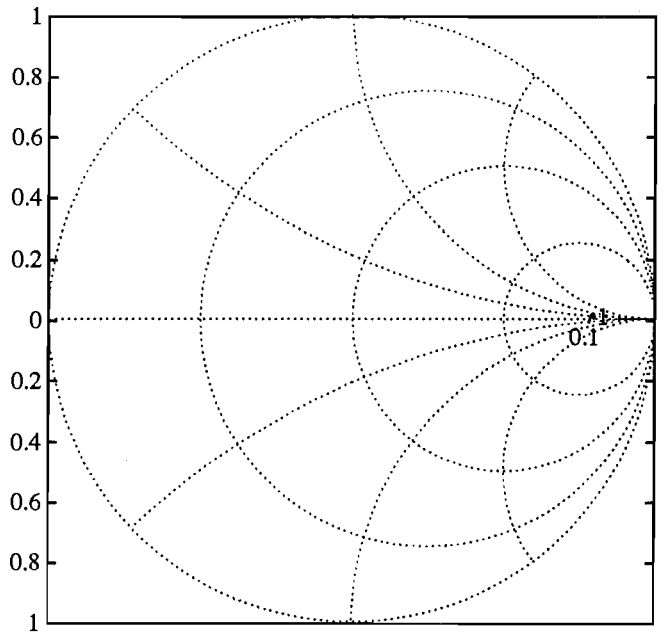


(a)

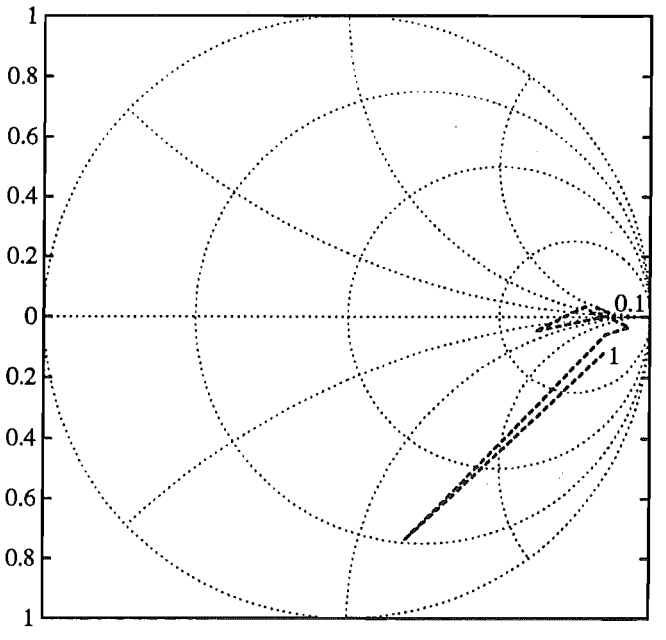


(b)

Figure E.8 FDR measurement results for R_3: 146 Ω (a) ANA results (b) FDR results.

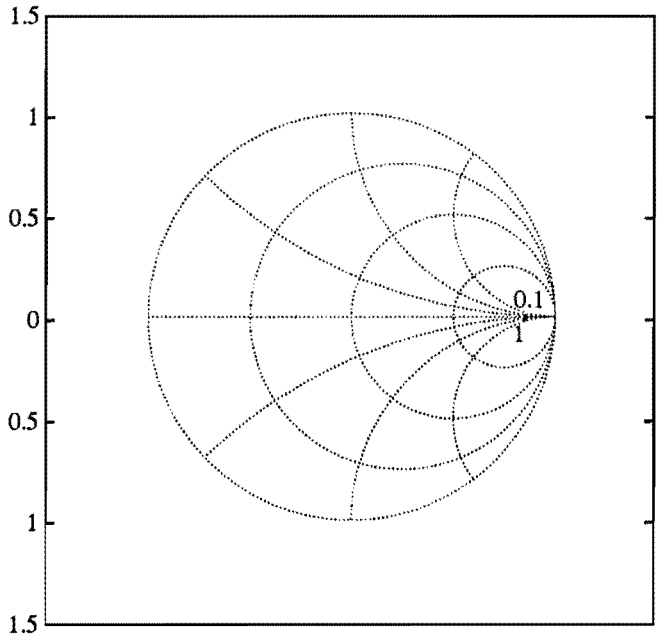


(a)

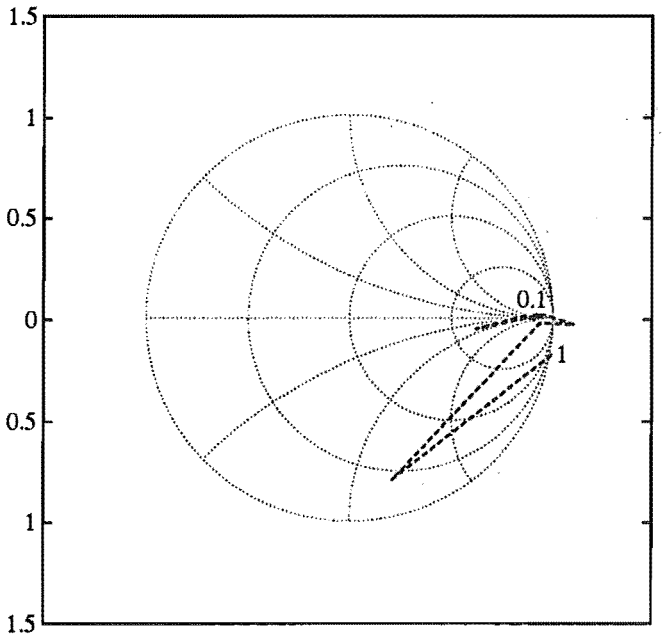


(b)

Figure E.9 FDR measurement results for R_4: 444 Ω (a) ANA results (b) FDR results.

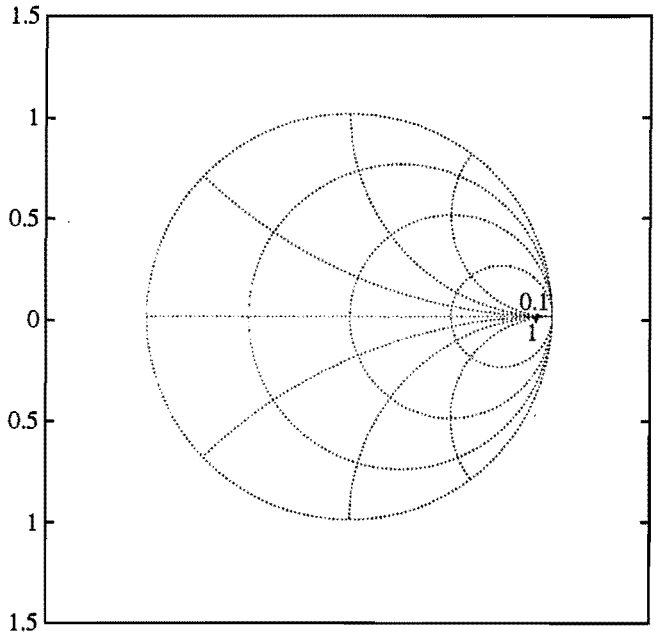


(a)

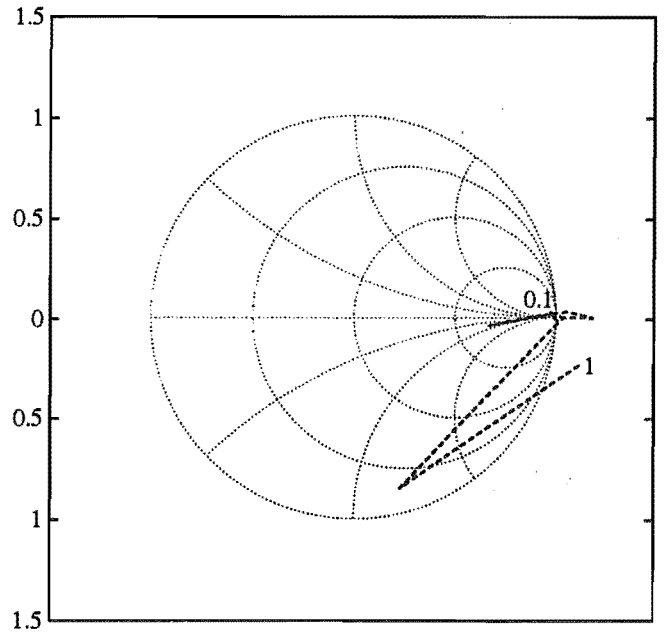


(b)

Figure E.10 FDR measurement results for R_5: 702 Ω (a) ANA results (b) FDR results.

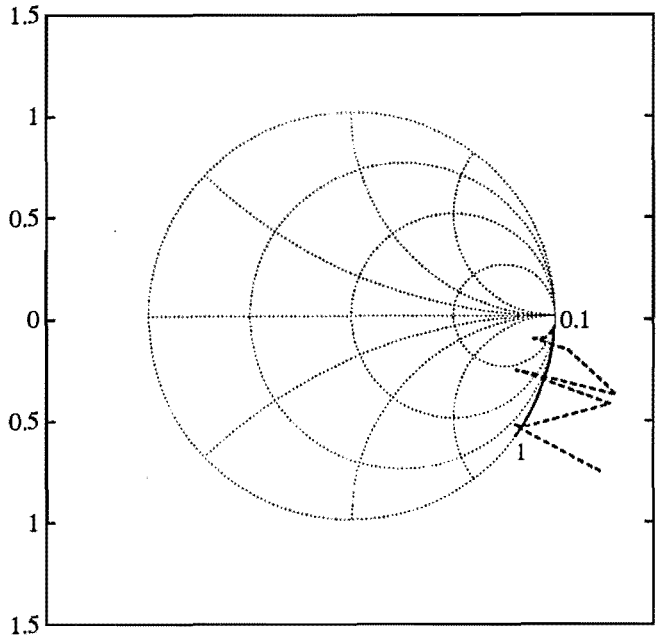


(a)

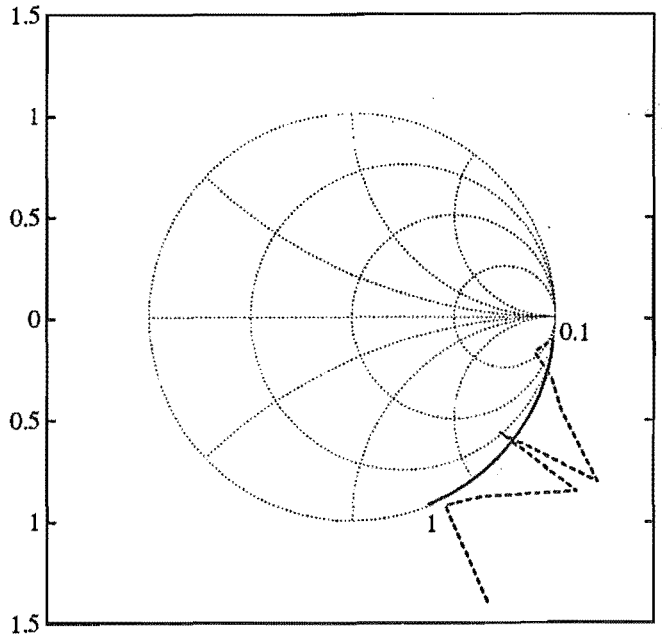


(b)

Figure E.11 FDR measurement results for R_6: 1.49 kΩ (a) ANA results (b) FDR results.

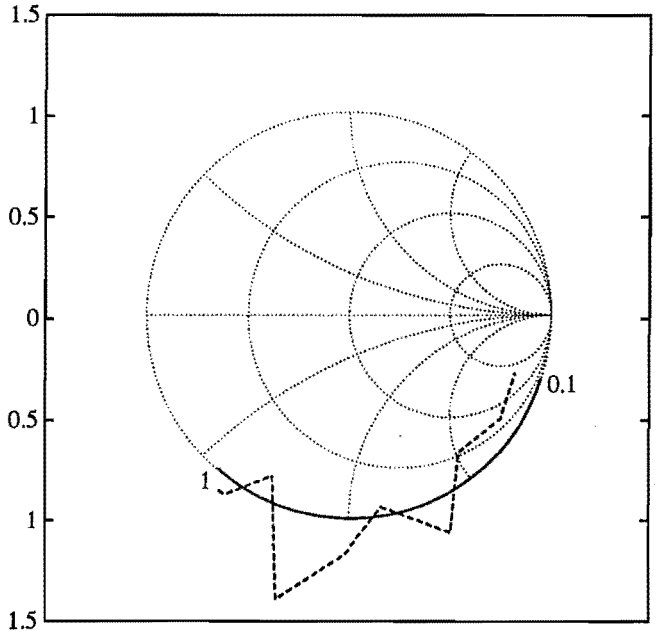


(a)

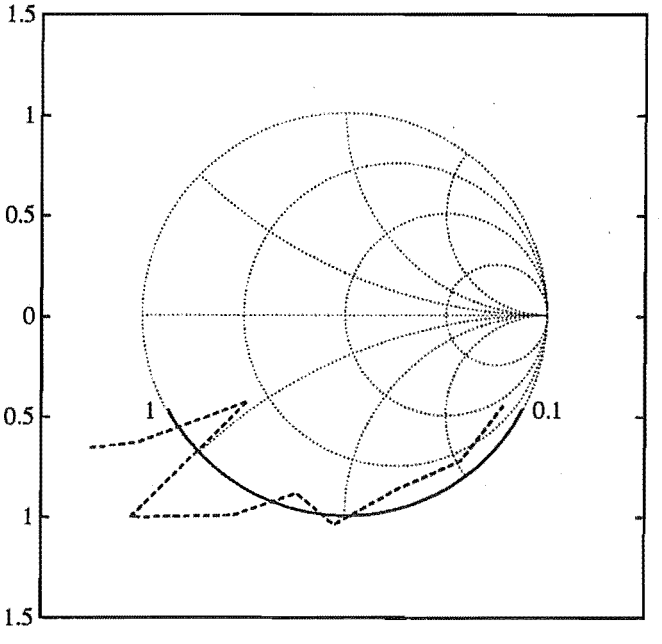


(b)

Figure E.12 FDR measurement results for (a) C_1: 1 pF (b) C_2: 2.2 pF.

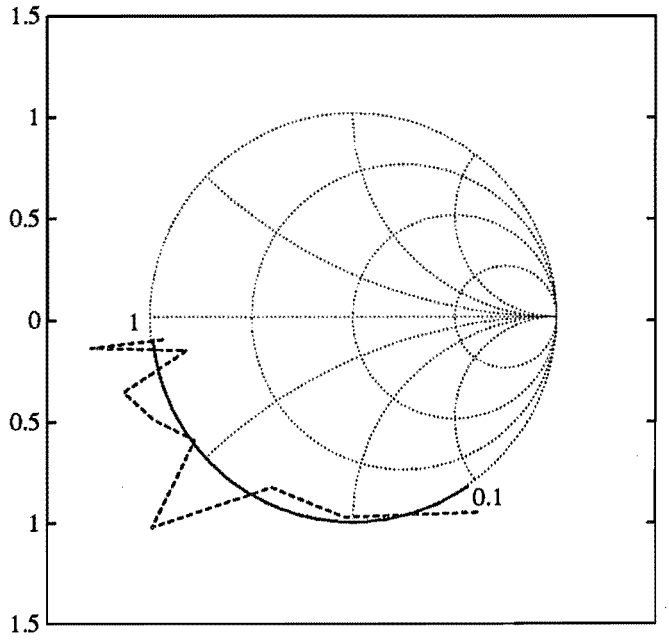


(a)

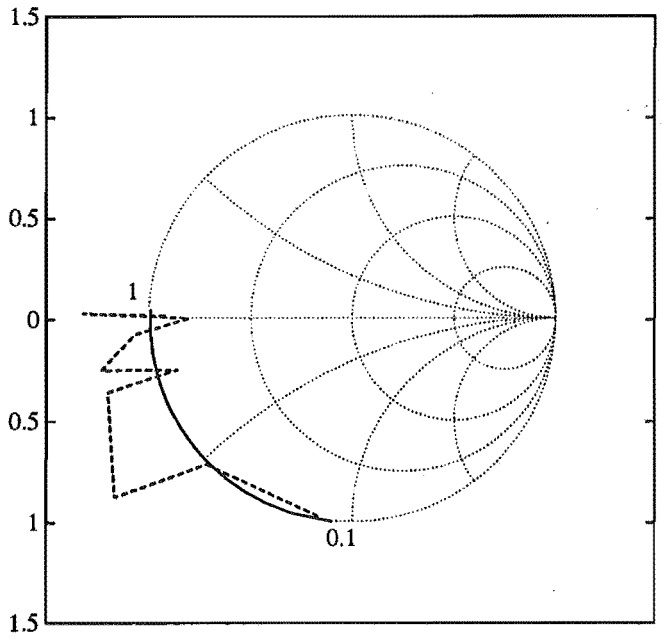


(b)

Figure E.13 FDR measurement results for (a) C_3: 4.7 pF (b) C_4: 8.2 pF.

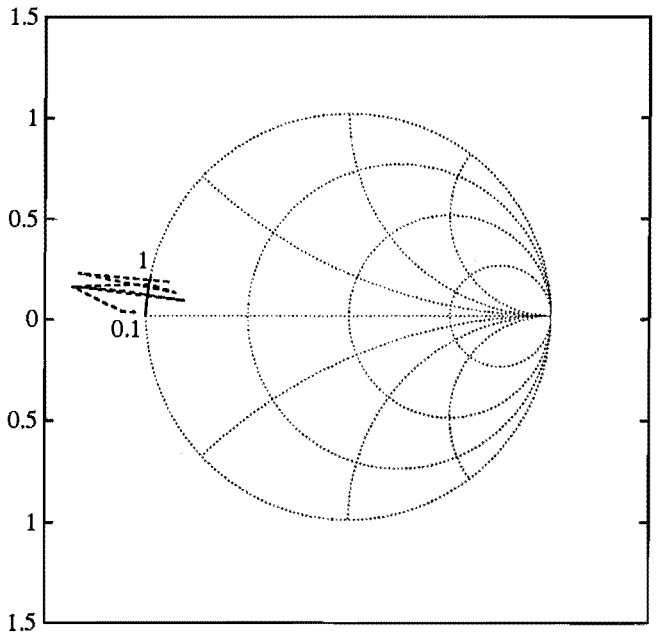


(a)

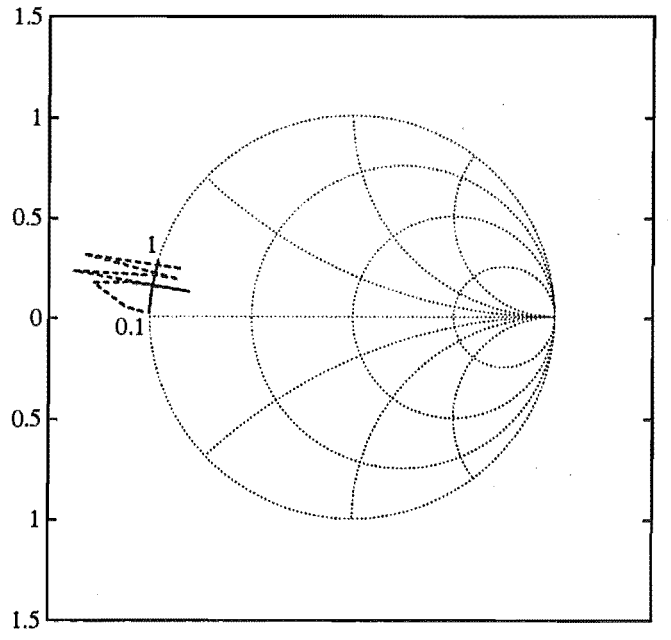


(b)

Figure E.14 FDR measurement results for (a) C_5: 18 pF (b) C_6: 33 pF.

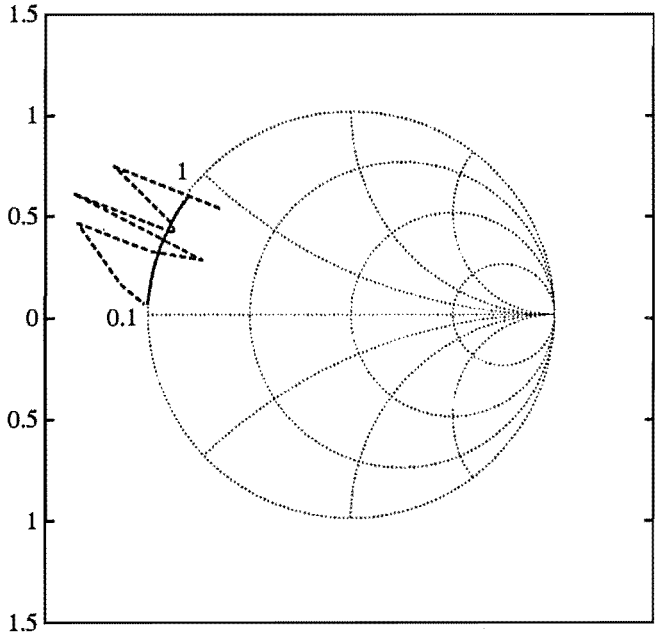


(a)

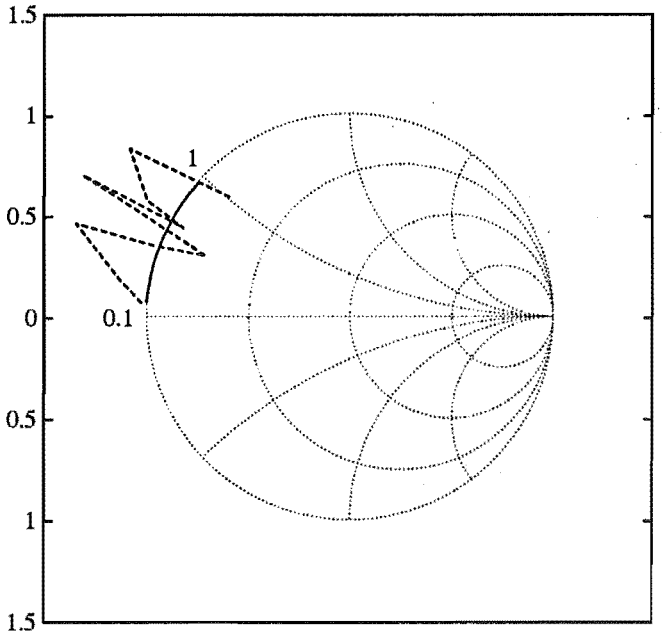


(b)

Figure E.15 FDR measurement results for (a) L_1: 0.68 nH (b) L_2: 1.92 nH.

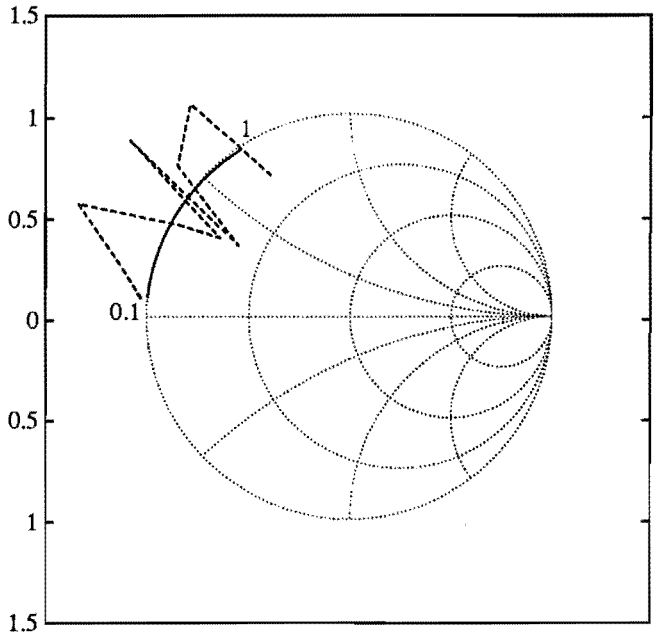


(a)

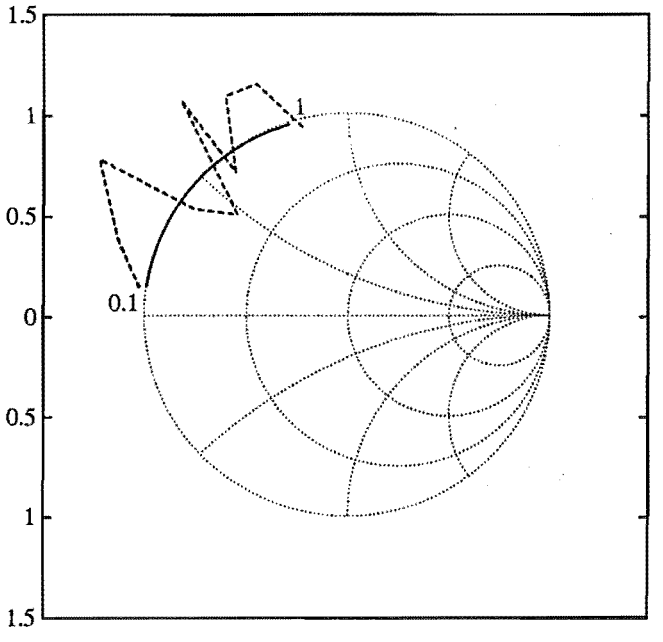


(b)

Figure E.16 FDR measurement results for (a) L_3: 3.37 nH (b) L_4: 4.95 nH.

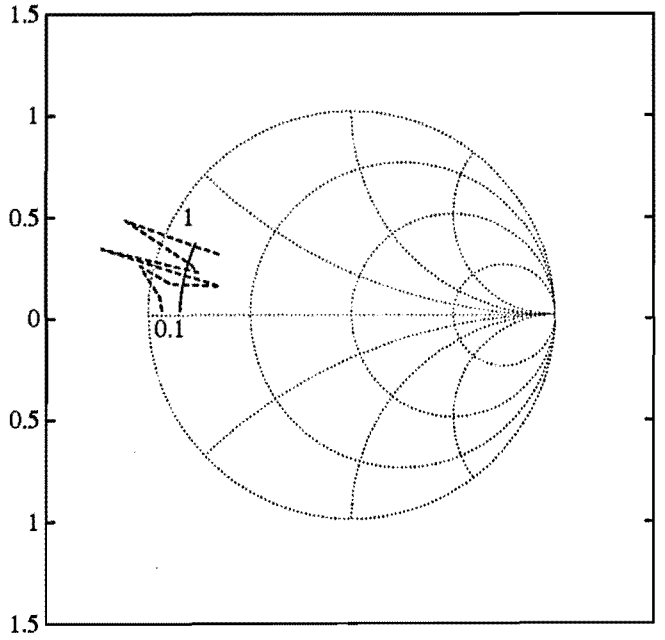


(a)

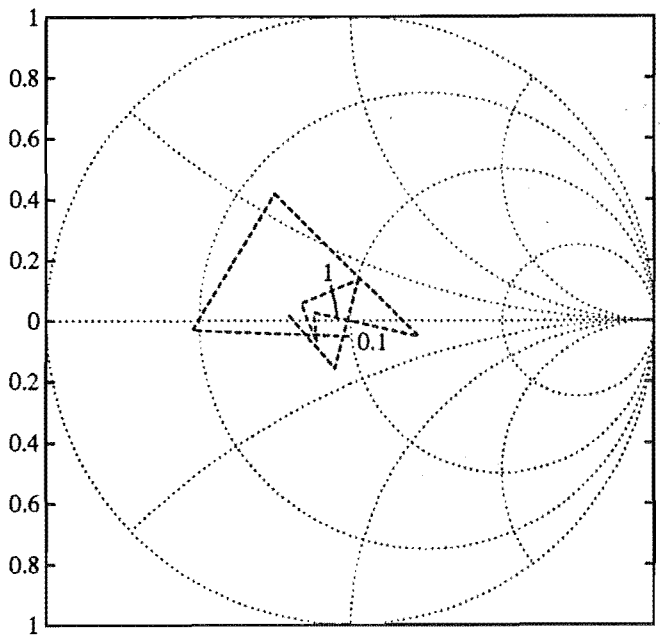


(b)

Figure E.17 FDR measurement results for (a) L_5: 6.63 nH (b) L_6: 8.4 nH.

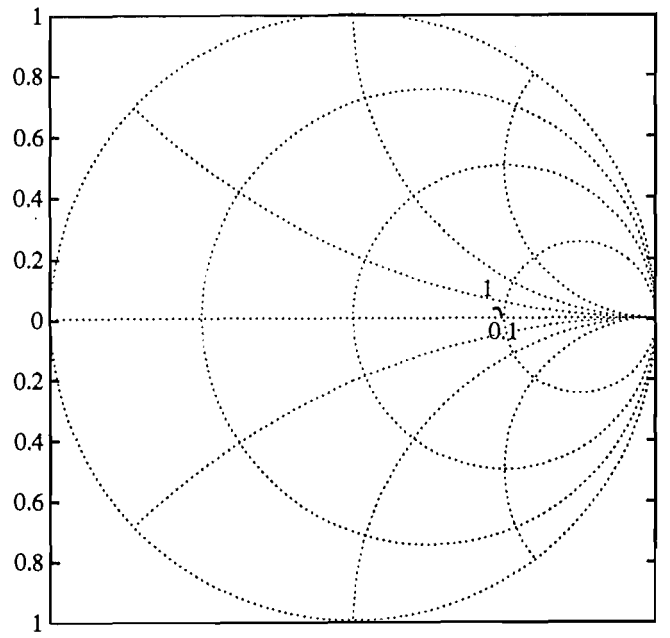


(a)

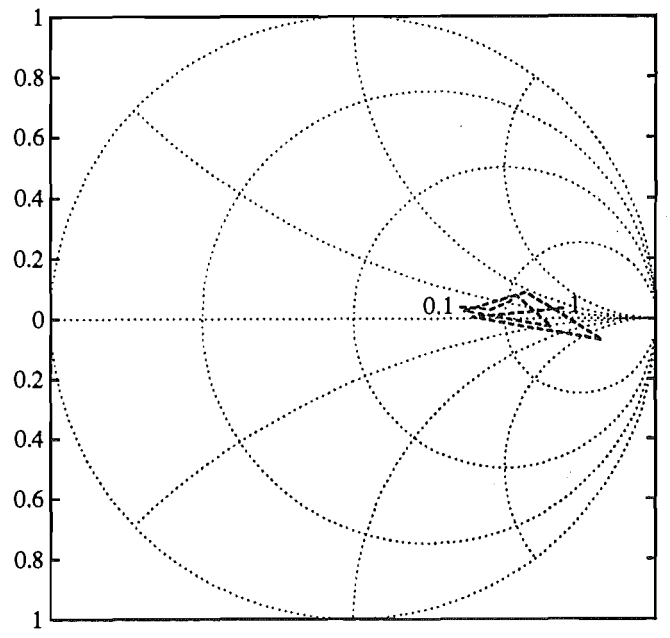


(b)

Figure E.18 FDR measurement results for (a) R_1: 4.4 Ω (b) R_2: 46 Ω.

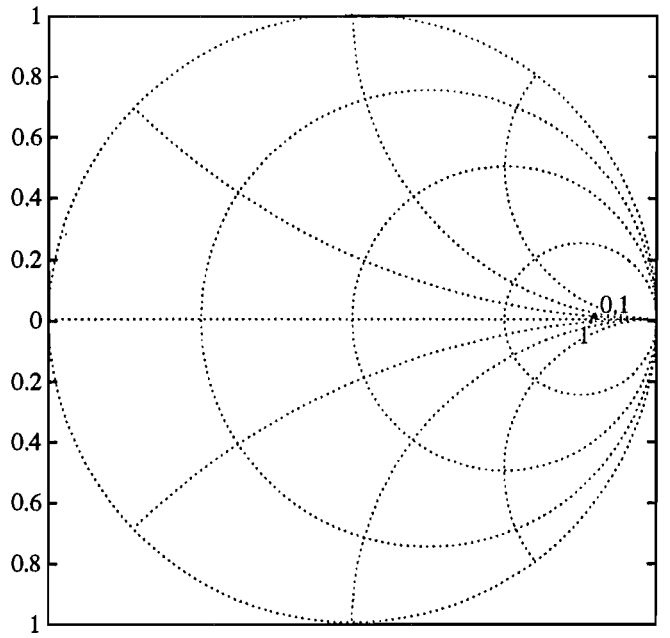


(a)

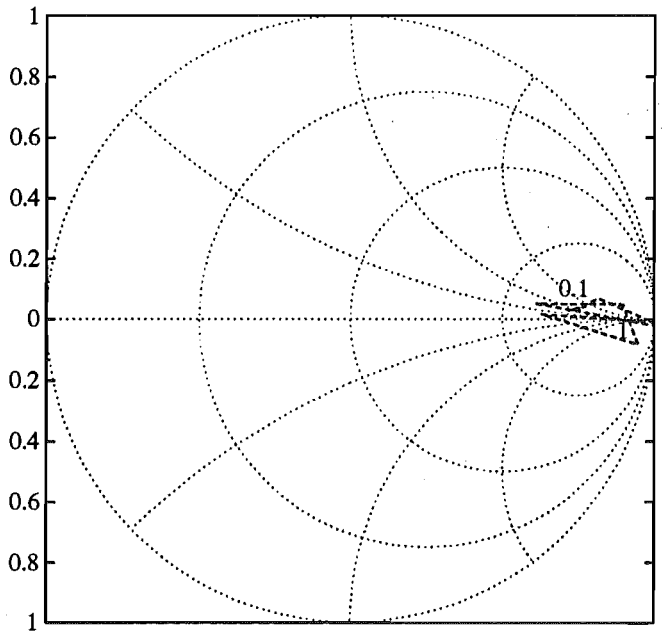


(b)

Figure E.19 FDR measurement results for R_3: 146 Ω (a) ANA results (b) FDR results.

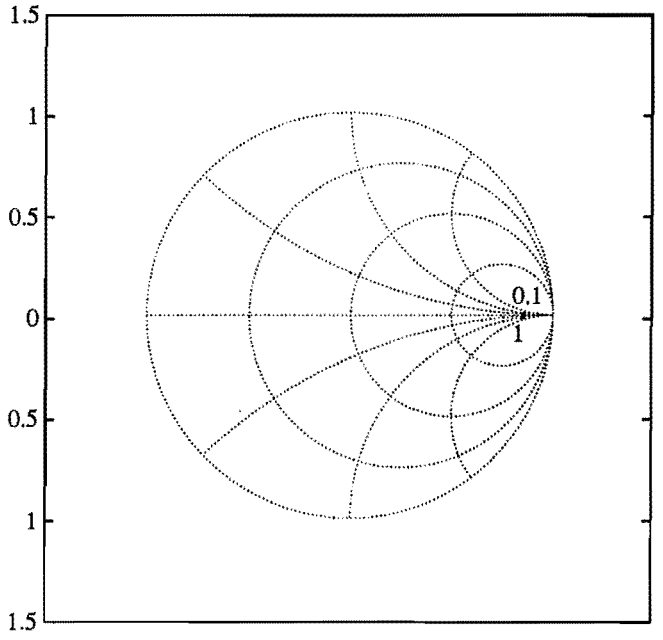


(a)

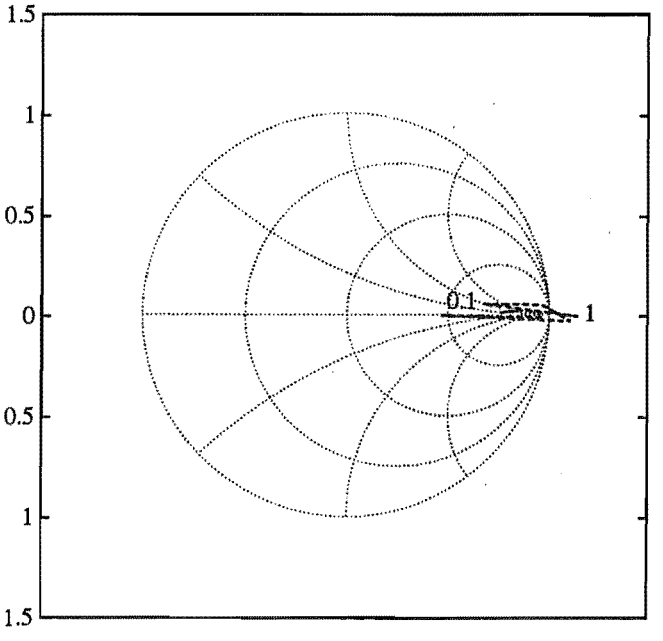


(b)

Figure E.20 FDR measurement results for R_4: 444 Ω (a) ANA results (b) FDR results.

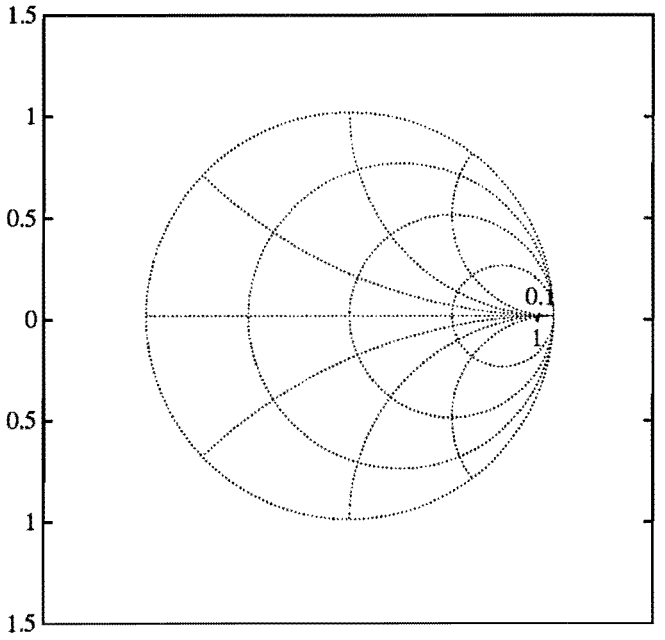


(a)

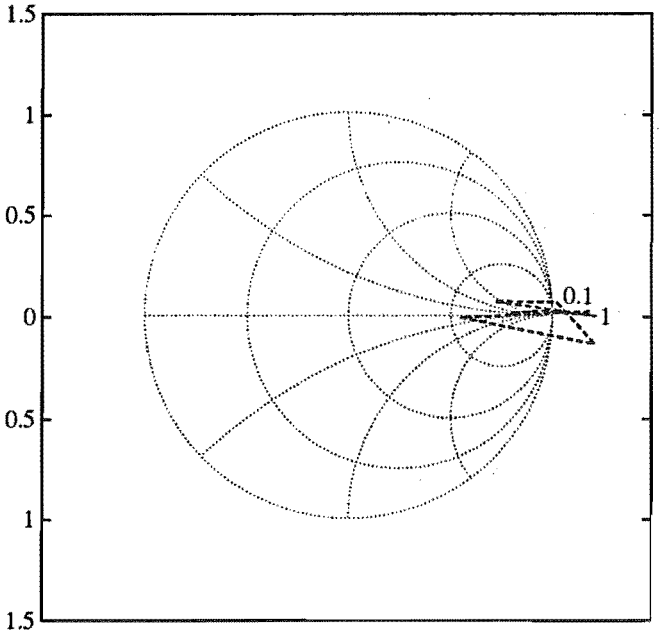


(b)

Figure E.21 FDR measurement results for R_5: 702Ω (a) ANA results (b) FDR results.



(a)



(b)

Figure E.22 FDR measurement results for R_6: 1.49 kΩ (a) ANA results (b) FDR results.

APPENDIX F

MAPLE PROCEDURES FOR SYMBOLIC COMPUTATION

The following procedures are MAPLE procedures for symbolic computation of signal flow graph reduction and $S \Leftrightarrow T$ matrix transformation.

F.1 SIGNAL FLOW GRAPH REDUCTION

```
gr_red := proc()
 local i,j,k,G,N;
 if nargs = 0 then
    ERROR('no arguments specified')
 else
   G := args[1];
   N := linalg[rowdim](G);
     for k from 1 to N-1 do
        for i from k+1 to N do
            if G[i,k] <> 0 then
               for j from k+1 to N do
                   if G[k,j] <> 0 then
                      G[i,j] := G[i,j]+(G[i,k]*G[k,j]/(1-G[k,k]))
                   fi;
               od;
            fi;
        od;
     od;
   RETURN(G[N,N]);
 fi;
end:
```

F.2 SCATTERING TO TRANSFER SCATTERING MATRIX TRANSFORMATION

```
S2T := proc()
local S;
if nargs = 0 then
   ERROR('No arguments specified')
else
S := args[1];
RETURN(array([[normal((S[1,2]*S[2,1]-S[1,1]*S[2,2])/S[2,1]),
normal(S[1,1]/S[2,1])],[normal(-S[2,2]/S[2,1]),normal(1/S[2,1])]]));
fi;
end:
```

F.3 TRANSFER SCATTERING TO SCATTERING MATRIX TRANSFORMATION

```
T2S := proc()
local T;
if nargs = 0 then
   ERROR('No arguments specified')
else
T := args[1];
RETURN(array([[normal(T[1,2]/T[2,2]),
normal((T[1,1]*T[2,2]-T[1,2]*T[2,1])/T[2,2])],
[normal(1/T[2,2]),normal(-T[2,1]/T[2,2])]]));
fi;
end:
```

APPENDIX G

SPICE INPUT FILES

The followings are three examples of SPICE version 2G.6 input files, used to simulate the nonlinear effects, computed and approximated compensation waveforms for the matched channel. Similar files, with transmission line characteristic impedance of 75 Ω, simulate the mismatched channel.

G.1 THE NONLINEAR EFFECTS

```
NONLINEAR EFFECTS
VIN 99  0 PULSE(0 5.0 0NS 0NS 0NS 10NS 20NS)
RS 99 98 50
CS 98 0 9PF
**** Assume ideal pin driver
**** Driver output impedance 50 ohms
EIN 97 0 98 0 1
R1 97 1 50
C1 1 0 5PF
**** PEC capacitor  and stray capacitor at connection
T1 1 0 2 0 Z0=50 TD=2NS
**** Transmission line from PEC to DUT
C2 2 0 5PF
L1 2 3 0.005UH
**** Inductance of conductor line in the package
**** from socket to chip bonding pad
CPAD 3 0 1PF
**** Linear load model for a DUT input pad
EIN2 96 0 98 0 1
R12 96 11 50
C12 11 0 5PF
**** PEC capacitor  and stray capacitor at connection
T12 11 0 12 0 Z0=50 TD=2NS
```

```
**** Transmission line from PEC to DUT
C22 12 0 5PF
L12 12 13 0.005UH
**** Inductance of conductor line in the package
**** from socket to chip pad
CPAD2 13 0 1PF
DPAD1 0 13 DIODE2
**** Power supply for CMOS inverter
VDD 66 0 DC 5
**** CMOS inverter (5 micron technology) subcircuit
.SUBCKT CINV 1 2 3 4 5
M1 2 1 4 4 NENH L=5U W=10U AS=100P AD=100P PD=40U
+PS=40U NRS=1.0 NRD=1.0
M2 2 1 3 5 PENH L=5U W=25U AS=250P AD=250P PD=70U
+PS=70U NRS=0.4 NRD=0.4
.ENDS CINV
**** connect an inverter as a load through
**** an input protection circuit
D1 0 13 DIODE
D2 13 66 DIODE
D3 0 14 DIODE
D4 14 66 DIODE
RP1 13 14 400
D5 14 66 DIODE
RP2 14 15 400
X1 15 16 66 0 66 CINV
CLOAD 16 0 1PF
**** Linear load model for a DUT input pad + nonlinear loads
*** Devices' models
.MODEL DIODE D(IS=1.5E-15 RS=0.5 TT=0.01NS CJO=0.8PF
+VJ=0.6 BV=40 IBV=10MA)
.MODEL DIODE2 D(IS=1.0E-14 RS=0.5 TT=10NS CJO=1PF VJ=0.8)
.MODEL NENH NMOS(LEVEL=2 VTO=1.0 KP=20E-6 GAMMA=0.347
+NSUB=5E14 TOX=0.1U XJ=1.0U LD=1.0U CJ=70U CJSW=220P
+CGSO=345P CGDO=345P RSH=30)
*** P transistor is formed in N WELL
*** therefore higher junction capacitances
.MODEL PENH PMOS(LEVEL=2 VTO=-1.5 KP=10E-6 GAMMA=0.275
+NSUB=8E14 TOX=0.1U XJ=1.0U LD=1.0U CJ=89U CJSW=278P
+CGSO=345P CGDO=345P RSH=30)
*** Comparison between DIODE and DIODE2
```

```
*** DIODE2 has larger junction area than DIODE (higher IS)
*** DIODE2 junction capacitor CJO is larger because N WELL
*** is more heavily doped than the substrate
*** DIODE2 built-in potential VJ is higher for the same reason
*** (VJ is proportional to doping concentration and temperature)
*** DIODE2 is a long-base diode (longer TT), but DIODE is a
*** short-base diode
.OPTIONS ITL3=8 ITL4=20 ITL5=8000 LIMPTS=20000
.TRAN 0.02NS 20NS
**** Analysis specification
.PRINT TRAN V(97) V(3) V(13)
**** Output
.END
```

G.2 COMPUTED COMPENSATION WAVEFORM FOR THE MATCHED CHANNEL

```
MATCHED LINE COMPENSATION
VIN 99  0 PULSE(0 5.25 2.72NS 0NS 0NS 10NS 20NS)
RS 99 98 50
CS 98 0 9PF
** Basic Pin driver output scaled up by 1/0.9524 delayed by 2.72 ns
EIN 97 96 98 0 1
VIN2 96 0 PWL(   0.0NS  0.0019  0.2NS  0.0925  0.4NS  -0.0484
+0.6NS  -0.0885  0.8NS  0.0936  1.0NS  0.0907  1.2NS  -0.1512
+1.4NS  -0.0981  1.6NS  0.2515  1.8NS  0.1291  2.0NS  -0.4804
+2.2NS  -0.2554  2.4NS  1.6028  2.6NS  3.8932  2.8NS   4.8009
+3.0NS   4.0287  3.2NS  2.6577  3.4NS  1.5690  3.6NS   0.9162
+3.8NS   0.6246  4.0NS  0.5344  4.2NS  0.3520  4.4NS   0.0449
+4.6NS  -0.0488  4.8NS  0.1466  5.0NS  0.2220  5.2NS   0.0068
+5.4NS  -0.1189  5.6NS  0.0416  5.8NS  0.1394  6.0NS  -0.0339
+6.2NS  -0.2130  6.4NS -0.2744  6.6NS -0.4006  6.8NS  -0.4057
+7.0NS   0.1741  7.2NS  1.0464  7.4NS  1.2435  7.6NS   0.6018
+7.8NS   0.0986  8.0NS  0.2847  8.2NS  0.4976  8.4NS   0.1763
+8.6NS  -0.1760  8.8NS -0.0285  9.0NS  0.2197  9.2NS   0.0811
+9.4NS  -0.1377  9.6NS -0.0396  9.8NS  0.1061 10.0NS  -0.0019
+10.2NS  -0.0925 10.4NS  0.0484 10.6NS  0.0885 10.8NS  -0.0936
+11.0NS  -0.0907 11.2NS  0.1512 11.4NS  0.0981 11.6NS  -0.2515
+11.8NS  -0.1291 12.0NS  0.4804 12.2NS  0.2554 12.4NS  -1.6028
+12.6NS  -3.8932 12.8NS -4.8009 13.0NS -4.0287 13.2NS  -2.6577
+13.4NS  -1.5690 13.6NS -0.9162 13.8NS -0.6246 14.0NS  -0.5344
```

```
+14.2NS  -0.3520 14.4NS -0.0449 14.6NS  0.0488 14.8NS  -0.1466
+15.0NS  -0.2220 15.2NS -0.0068 15.4NS  0.1189 15.6NS  -0.0416
+15.8NS  -0.1394 16.0NS  0.0339 16.2NS  0.2130 16.4NS   0.2744
+16.6NS   0.4006 16.8NS  0.4057 17.0NS -0.1741 17.2NS  -1.0464
+17.4NS  -1.2435 17.6NS -0.6018 17.8NS -0.0986 18.0NS  -0.2847
+18.2NS  -0.4976 18.4NS -0.1763 18.6NS  0.1760 18.8NS   0.0285
+19.0NS  -0.2197 19.2NS -0.0811 19.4NS  0.1377 19.6NS   0.0396
+19.8NS  -0.0169 20.0NS  0.0019 )
** Constructing Pin driver output + computed compensation waveforms
R1 97 1 50
**** Driver output impedance 50 ohms
C1 1 0 5PF
**** PEC capacitor and stray capacitor at connection
T1 1 0 2 0 Z0=50 TD=2NS
**** Matched transmission line from PEC to DUT
C2 2 0 5PF
**** Stray capacitor at socket connection
RL 3 0 1K
LL 2 3 0.005UH
CL 3 0 10PF
**** Load model for an input pin of the DUT
.OPTIONS ITL3=8 ITL4=20 ITL5=8000 LIMPTS=20000
.IC V(3) = 0 V(2) = 0
.TRAN 0.02NS 30NS UIC
**** Analysis specification
.PRINT TRAN V(97) V(3)
**** Print Pin Driver output and DUT input waveforms
.END
```

G.3 APPROXIMATED COMPENSATION WAVEFORM FOR THE MATCHED CHANNEL

```
MATCHED LINE COMPENSATION
VIN 99  0 PULSE(0 5.25 2.72NS 0NS 0NS 10NS 20NS)
RS 99 98 50
CS 98 0 9PF
** Basic Pin driver output scaled up by 1/0.9524 delayed by 2.72 ns
VIN2 88  0 PULSE(0 6.829 2.26NS 0NS 0NS 10NS 20NS)
RS2 88 87 50
CS2 87 0 8.3656PF
VIN3 78  0 PULSE(0 6.829 2.82NS 0NS 0NS 10NS 20NS)
```

```
RS3 78 77 50
CS3 77 0 10.34PF
VIN4 68  0 PULSE(0 1.4827 6.92NS 0NS 0NS 10NS 20NS)
RS4 68 67 50
CS4 67 0 12.7114PF
VIN5 58  0 PULSE(0 1.4827 7.34NS 0NS 0NS 10NS 20NS)
RS5 58 57 50
CS5 57 0 15.2344PF
**** Approximated compensation waveforms
EIN 97 96 98 0 1
EIN2 96 95 87 0 1
EIN3 95 94 77 0 -1
EIN4 94 93 67 0 1
EIN5 93 0 57 0 -1
**** Constructing Pin driver output using VCVS
R1 97 1 50
**** Driver output impedance 50 ohms
C1 1 0 5PF
**** PEC capacitor and stray capacitor at connection
T1 1 0 2 0 Z0=50 TD=2NS
**** Matched transmission line from PEC to DUT
C2 2 0 5PF
**** Stray capacitor at socket connection
RL 3 0 1K
LL 2 3 0.005UH
CL 3 0 10PF
**** Load model for an input pin of the DUT
.OPTIONS ITL3=8 ITL4=20 ITL5=8000 LIMPTS=20000
.IC V(3) = 0 V(2) = 0
.TRAN 0.02NS 30NS UIC
**** Analysis specification
.PRINT TRAN V(97) V(3)
**** Print Pin Driver output and DUT input waveforms
.END
```

APPENDIX H

THE CHANNEL GENERAL EQUATION

The general equation for a uniform lossless transmission path is:

$$H(s) = \frac{H_N(s)}{H_{D1}(s) + H_{D2}(s) + H_{D3}(s) + H_{D4}(s) + H_{D5}(s)} \tag{H.1}$$

where

$$H_N(s) = 2Y_0\left(\rho_T^2 - 1\right)(RY_0 + sRC + 1)e^{-s\tau} \tag{H.2}$$

$$\begin{aligned} H_{D1}(s) = {} & s^4\left(2RCC_1C_2L\rho_T - RCC_1C_2L\rho_T^2 - RCC_1C_2L\right) \\ & + s^4e^{-2s\tau}\left(RCC_1C_2L\rho_T^2 - 2RCC_1C_2L\rho_T + RCC_1C_2L\right) \end{aligned} \tag{H.3}$$

$$\begin{aligned} H_{D2}(s) = {} & s^3\left(2C_1C_2L\rho_T - C_1C_2L\rho_T^2 - C_1C_2L - 2RCC_2LY_0\right. \\ & \left. + RCC_1L\rho_T^2Y_0 - RCC_1LY_0 + 2RCC_2L\rho_TY_0\right) \\ & + s^3e^{-2s\tau}\left(2RCC_2L\rho_T^2Y_0 - RCC_1LY_0 - 2RCC_2L\rho_TY_0\right. \\ & \left. + RCLC_1\rho_T^2Y_0 - 2C_1C_2L\rho_T + C_1C_2L + C_1C_2L\rho_T^2\right) \end{aligned} \tag{H.4}$$

$$\begin{aligned} H_{D3}(s) = {} & s^2\left(C_1L\rho_T^2Y_0 + 2C_2L\rho_TY_0 - LC_1Y_0 - 2C_2LY_0 + 2RCC_1\rho_T - RCC_1\rho_T^2\right. \\ & \left. + 2RC_1C_2\rho_T - 2RCL\rho_TY_0^2 - 2RCLY_0^2 - RC_1C_2\rho_T^2 - RCC_1 - RC_1C_2\right) \\ & + s^2e^{-2s\tau}\left(RC_1C_2 + RCC_1 + RCC_1\rho_T^2 + RC_1C_2\rho_T^2 - 2RCC_1\rho_T\right. \\ & -2RC_1C_2\rho_T + 2RCL\rho_TY_0^2 + 2RCL\rho_T^2Y_0^2 - C_1LY_0 - 2C_2L\rho_TY_0 \\ & \left. + 2C_2L\rho_T^2Y_0 + C_1L\rho_T^2Y_0\right) \end{aligned} \tag{H.5}$$

$$\begin{aligned} H_{D4}(s) = {} & s\left(2C_1\rho_T - C_1 - 2LY_0^2 - C_1\rho_T^2 - 2RCY_0 + 2RC\rho_TY_0\right. \\ & \left. + RC_1\rho_T^2Y_0 - 2RC_2Y_0 + 2RC_2\rho_TY_0 - RC_1Y_0 - 2L\rho_TY_0^2\right) \\ & + se^{-2s\tau}\left(2RC\rho_T^2Y_0 - RC_1Y_0 + C_1\rho_T^2 + C_1 - 2C_1\rho_T\right. \\ & \left. -2RC\rho_TY_0 + RC_1\rho_T^2Y_0 - 2RC_2\rho_TY_0 + 2L\rho_T^2Y_0^2 + 2L\rho_TY_0^2 + 2RC_2\rho_T^2Y_0\right) \end{aligned} \tag{H.6}$$

$$\begin{aligned} H_{D5}(s) &= 2Y_0\left(\rho_T - R\rho_T Y_0 - RY_0 - 1\right) \\ &\quad +2\rho_T Y_0 e^{-2sT}\left(\rho_T + R\rho_T Y_0 + RY_0 - 1\right) \end{aligned} \tag{H.7}$$

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